

# The Bifet Design Manual

1984/85

**General Purpose, Low Noise,  
Low Power, Low Offset**



**TEXAS  
INSTRUMENTS**



# The Bifet Design Manual

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## 1. INTRODUCTION

This manual is intended to be used as a convenient reference work for a wide range of analogue circuit and system designs. It has been compiled from a large number of individual applications, each of which has been classified under a general heading along with others of a similar nature. The report includes sections on amplification, sampling, filter and oscillator circuits as well as data on individual devices and a section on miscellaneous circuits.

For each application the report gives a full circuit diagram, design equations and a description of the circuit operation. In addition, in many cases the derivation of the design equations has been given in an attempt to impart a fuller understanding of the circuit operation. It was felt that this was a worthwhile departure from the usual procedure of merely quoting seemingly "magical" design or performance equations without further explanation. The derivations can also be used as the basis for design modifications to produce a circuit which is more exactly compatible with a particular application.

Throughout the report the operational amplifiers used have been selected from the Texas Instruments BIFET range. This has enabled the design equations to be simplified considerably and the circuit performance enhanced, since in most cases the circuit performance limitations are not directly related to the op amp performance in terms of bias currents, input impedance, speed etc., as is usually the case. Consequently the applications can often be duplicated using conventional op amps provided that care is taken to see that significant effects caused by the op amp itself are comprehended in the re-worked design equations

The applications and circuit diagrams themselves are fairly self-explanatory. It is assumed that the reader is familiar with the usual terms relating to operational amplifiers (op amps) such as inverting and non-inverting inputs (or - ve and + ve inputs), slew rate, offset voltages etc. It has also been assumed that throughout the report, unless stated otherwise, the operational amplifiers are fed from a  $\pm 15V$  supply.

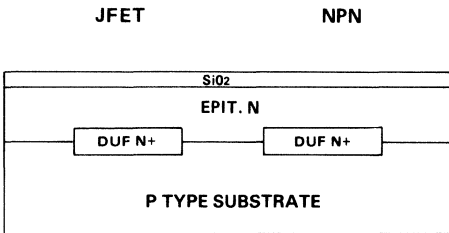
Acknowledgement is made to the many other people in Texas Instruments Ltd., Bedford, whose help and ideas have greatly added to the content and accuracy of this book.

## 2. WHAT IS A BIFET?

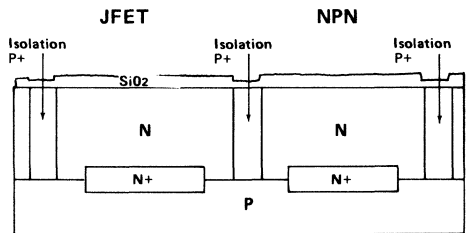
The term BIFET, as used in this manual, is a generic name referring to a range of Texas Instruments operational amplifiers with JFET input transistors. Perhaps more correctly BIFET is the name of the process used to manufacture such devices which as the name suggests involves the production of both JFET and bipolar transistors on a common substrate.

It has, of course, been possible to produce both JFETs and bipolar transistors together for many years although the problem has always been to produce sufficiently well matched pairs of FETS that would be required for the input stage of a high performance operational amplifier. In the past matching could only be achieved by changing the individual bias on the input transistor during processing, usually by a technique known as "Zener Zapping". This is a difficult and time consuming exercise which is reflected in the price of the final device.

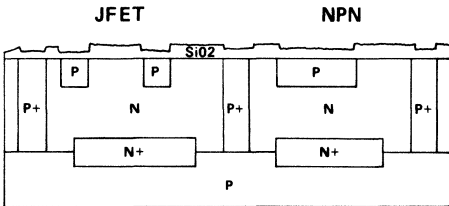
Starting substrate with N<sup>+</sup> Diffusion and N-type epitaxial layer



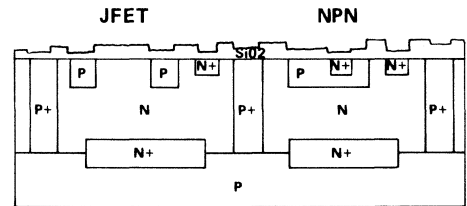
Isolation diffusion



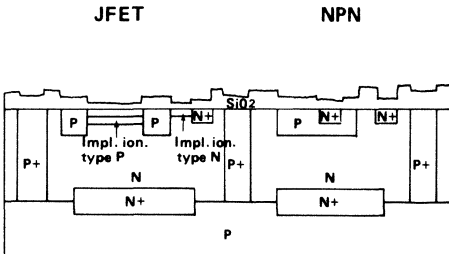
Formation of JFET drain and source and NPN base



NPN emitter and collector and JFET gate formation



JFET gate implants



Metalization

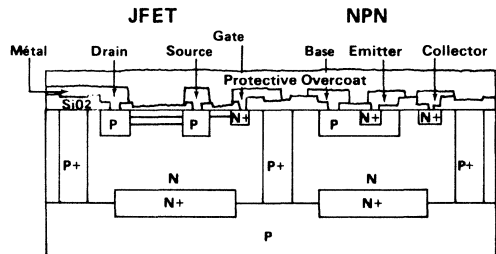


Fig. 2.1 BIFET Process



In the Texas Instruments BIFET process matched FETS are produced by a technique known as Ion Implantation. This is a technique whereby different types of semiconductor material are produced not by the diffusion of impurities but by the bombardment of ions from an ion source. The area not to be implanted is masked with a layer of oxide, metal or photoresist. The masking techniques are the same ones used in the conventional technology for making silicon integrated circuits. The advantage of the method lies in the accuracy with which the implantation can be controlled and also the uniformity of the implantation over the full area of the wafer. In this way JFETs may be produced being closely matching in terms of gain and pinch-off voltage. i.e. ideally suited to be the input devices of an operational amplifier.

The various stages of the BIFET process is shown in fig. 2.1.

The range of Texas Instruments BIFET operational amplifiers can be divided into three main families. In general each family includes a single, dual and quad version as well as a single with provision for external compensation.

The TL080 series have been designed as general purpose op amps. It combines a low distortion bipolar output stage with the advantages of JFET input transistors (low bias current and high input impedance).

The TL070 series is similar to the general purpose TL080 series but with low noise characteristics. This makes members of this series ideal for use in high performance, low noise applications.

The TL060 series is again similar to the TL080 series but incorporates a trade off of slew rate for minimal power dissipation. A variation of this is the TL066 which offers a programmable power option. These devices were designed for battery operation and other applications requiring a minimum of power dissipation combined with the performance characteristics of a BIFET operational amplifier.

To explain the operation of all these devices Fig. 2.2 gives the basic circuit diagram relating to the TL070/80 series, as an example.

The epitaxial FET Q16 acts as a current source feeding zener diode D2 which produces a voltage of 5.2V on the base of Q15. This results in a constant current source which is "mirrored" by Q14, Q9 and Q1 to provide bias currents for the input and second stages. The zener voltage of D2 controls the minimum supply voltage at which the device functions correctly, which is typically 6V.

The JFET input transistors, Q2 and Q3 operate into an active load consisting of Q4, Q6 and Q7. Current imbalance and input offset voltages may be adjusted on the TL081, TL071 and TL083 through connections to the emitter of Q6 and Q7, External offset controls for the TL080 and TL070 connect the collector of Q6 and Q7.

The compensation capacitor C1, is internal on the TL081/071, TL082/72, TL083, TL084/74 and TL085/75. In the TL080/70 a connection is provided for external compensation adjustment.

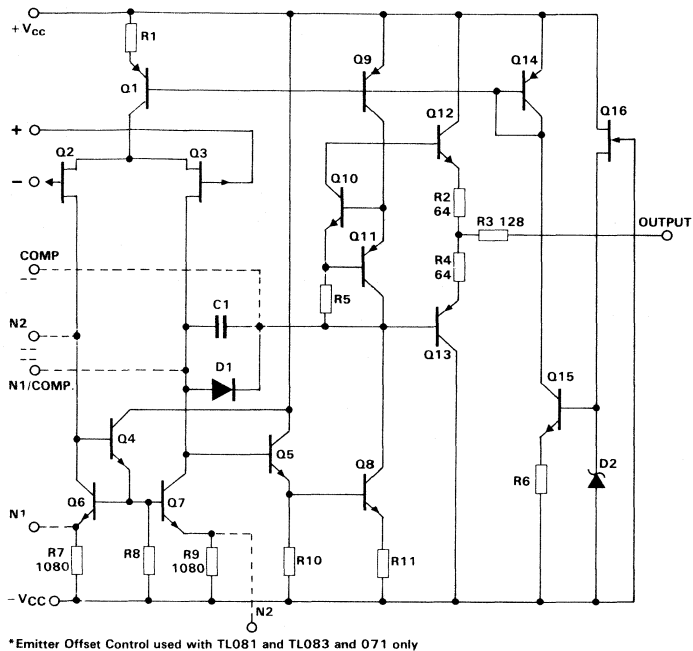


Fig. 2.2 TL071 & TL081

The Ion-Implanted input devices provide low bias currents, controlled pinch-off voltages for maximum common-mode input range and matched characteristics to minimise the input offset voltage. JFET inputs also offer the advantage of a comparatively high drive to the second stage producing a high output voltage swing capability and a wide power bandwidth.

Drive from the input stage is single ended from the collector of Q7. D1 provides a clamping action across Q5 and Q8 preventing saturation of Q8 and excessive current in Q5. Q5 and Q8 form the high gain second stage which drives the output stage consisting of Q10, Q11, Q12 and Q13.

Q10 and Q11 bias the output transistor Q12 and Q13 into class AB operation. This produces near zero crossover distortion and produces a low total harmonic distortion at the output. R2, R3 and R4 form a simple but effective output short circuit protection network and this together with the uncomplicated output stage minimise the silicon area requirements and thus helps to keep the manufacturing costs down.

### 3. AMPLIFICATION CIRCUITS

This section deals with a number of applications where a BIFET may be used in some form of amplifier.

Instrumentation amplifiers are the first to be considered, then low noise applications of the TL070 series and finally the design of a logarithmic amplifier is discussed.

#### 3.1 Instrumentation Amplifier

An instrumentation amplifier is a general term used to describe an amplifier with a high impedance differential input and a single ended output. Applications for such an amplifier include differential voltage measurement, bridge output voltage measurement or measurement of low level signals.

3.1.1 Fig 3.1. shows the classical op amp circuit for a differential amplifier. In this example, as in those which follow, a TL066 adjustable low power BIFET op amp has been used. These allow the power consumption to be programmed

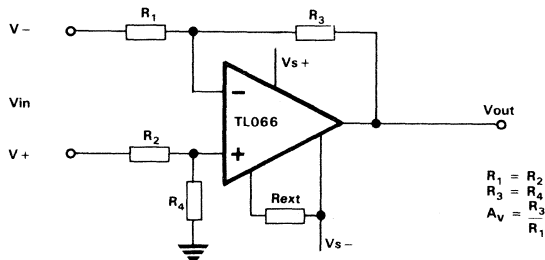


Fig. 3.1 Differential Amplifier

using a single external resistor,  $R_{ext}$ , to give a supply current between 5 and  $200\mu A$ . This can be a useful feature in an instrumentation amplifier as it allows a compromise between power consumption and bandwidth (and hence noise) to be achieved. If this feature is not required however the applications given in this section are equally applicable to any of the BIFET range.

The circuit shown in Fig. 3.1 may be analysed as follows.

$$\text{Gain from +ve input to output} = \frac{R_4}{R_2 + R_4} \times \left( 1 + \frac{R_3}{R_1} \right) \quad 1.$$

$$\text{Gain from -ve input to output} = -\frac{R_3}{R_1} \quad 2.$$

$$V_{out} = \frac{R_4}{R_2 + R_4} \times \left( 1 + \frac{R_3}{R_1} \right) \times V_+ - \frac{R_3}{R_1} \times V_- \quad 3.$$

If  $R_1 = R_2$  and  $R_3 = R_4$

$$\text{this becomes } \frac{R_3}{R_2 + R_3} \times \left( \frac{R_2 + R_3}{R_2} \right) V_+ - \frac{R_3}{R_2} V_- \quad 4.$$

$$V_{\text{out}} = (V_+ - V_-) \times \frac{R_3}{R_2} \quad 5.$$

The circuit as it stands has three main disadvantages:

- 1) The input impedance is comparatively low
- 2) The input impedance is different for the + ve and – ve inputs being equal to  $R_1$  for the inverting input and  $R_2 + R_4$  for the non-inverting input
- 3) The common mode rejection is effected greatly by the source impedances since this effectively alters the matching of the resistances (see below).

#### Common Mode Rejection

From equation 3 above for an applied common mode signal  $V = V_+ = V_-$

$$\frac{V_{\text{out}}}{V} = \left[ \frac{R_4}{R_2 + R_4} \left( 1 + \frac{R_3}{R_1} \right) - \frac{R_3}{R_1} \right] = \text{common mode gain} \quad 6.$$

If  $R_3 = R_4 = 100R_1$  but  $R_2 = 1.1 R_1$  due to mismatch

$$\frac{V_{\text{out}}}{V} = \frac{100R_1}{1.1R_1 + 100R_1} \left( 1 + \frac{100R_1}{R_1} \right) - \frac{100R_1}{R_1} \quad 7.$$

$$\frac{V_{\text{out}}}{V} = \frac{100}{101.1} \times 101 - 100 = -0.099$$

Common Mode Rejection Ratio (CMRR) is defined as:

$$\left| \frac{\text{Differential Gain}}{\text{Common Mode Gain}} \right| \approx \frac{100}{0.099} = 1010 \text{ or } \approx 60\text{dB}.$$

Thus a 10% mismatch has reduced the CMRR to approx 60dB.

**3.1.2** Fig. 3.2 shows a two op amp solution which overcomes two of the drawbacks listed above.

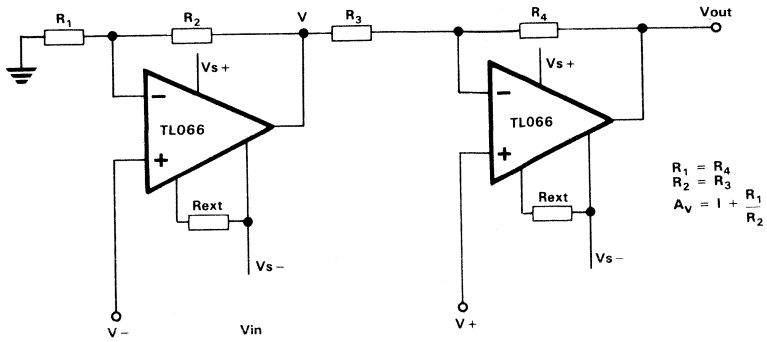


Fig. 3.2 Two Op Amp Instrumentation Amplifier

$$\begin{aligned} R_1 &= R_4 \\ R_2 &= R_3 \\ A_v &= 1 + \frac{R_1}{R_2} \end{aligned}$$

From Fig. 3.2  $\frac{V}{V_-} = 1 + \frac{R_2}{R_1}$ ,  $\frac{V_{out}}{V} = -\frac{R_4}{R_3}$

$$\therefore \frac{V_{out}}{V_-} = - \left( 1 + \frac{R_2}{R_1} \right) \times \frac{R_4}{R_3} \quad 8.$$

Also  $\frac{V_{out}}{V_+} = \left( 1 + \frac{R_4}{R_3} \right)$  9.

$$\therefore V_{out} = \left( 1 + \frac{R_4}{R_3} \right) V_+ - \left( 1 + \frac{R_2}{R_1} \right) \times \frac{R_4}{R_3} V_- \quad 10.$$

Thus if  $R_1 = R_4$  and  $R_2 = R_3$

$$V_{out} = (V_+ - V_-) \times \left( 1 + \frac{R_1}{R_2} \right) \quad 11.$$

An analysis of the common mode rejection shows the same performance as the earlier circuit.

Let  $V_- = V_+ = V$

$$\therefore V_{out} = \left[ \left( 1 + \frac{R_4}{R_3} \right) - \left( 1 + \frac{R_2}{R_1} \right) \times \frac{R_4}{R_3} \right] V \quad 12.$$

$$\therefore V_{out} = \left( 1 - \frac{R_2}{R_1} \times \frac{R_4}{R_3} \right) V \quad 13.$$

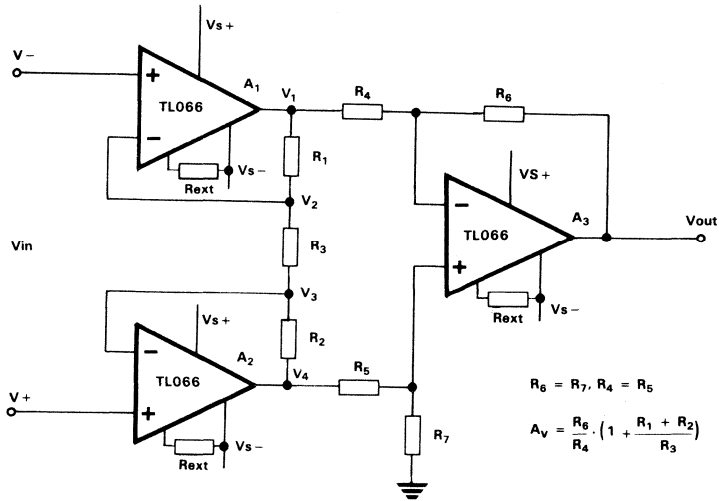
For constant test conditions, let  $R_1 = 99.R_2 \Rightarrow$  differential gain  $\approx 100$ ;  $R_3 = R_2$  but  $R_4 = 1.1 R_1$

$$\therefore \text{CMRR} = \left| \frac{100}{1 - \frac{R_2}{R_1} \times \frac{R_4}{R_3}} \right| = \frac{100}{1 - 1.1} = 1000 \text{ or } 60\text{dB} \quad 14.$$

Thus again a 10% mismatch has reduced the CMRR to approx. 60dB.

The main drawback of this circuit lies in its CMRR to a.c. signals. This is a result of an a.c. signal on the  $-V_e$  input being bandlimited by two op amps whilst the  $+V_e$  input signals need only need pass through one amplifier.

**3.1.3.** This limitation is overcome by the three op amp solution in Fig. 3.3.



*Fig. 3.3 Three Op Amp Instrumentation Amplifier*

Assume  $V_- = 0$ , then  $V_2 = 0$  and  $V_3 = V_+$

$$\therefore V_4 = V_+ \left( 1 + \frac{R_2}{R_3} \right) \quad 15.$$

$$\text{and } V_1 = - V_+ \times \frac{R_1}{R_3} \quad 16.$$

Similarly if  $V_+ = 0$ .

$$V_1 = V_- \left( 1 + \frac{R_1}{R_3} \right) \quad 17.$$

$$\text{and } V_4 = -V_- \times \frac{R_2}{R_3} \quad 18.$$

Therefore by superposition:

$$(V_4 - V_1) = (V_+ - V_-) \left( 1 + \frac{R_1 + R_2}{R_3} \right) \quad 19.$$

If  $R_6 = R_7$  and  $R_4 = R_5$ , then A3 functions as the basic differential amplifier thus

$$V_{out} = (V_+ - V_-) \times \frac{R_6}{R_4} \times \left( 1 + \frac{R_1 + R_2}{R_3} \right) \quad 20.$$

The matching of the network around A3 determines the CMRR as described previously. Since signals from both inputs have a similar path this circuit does not suffer from degradation of CMRR for a.c. signals. It also has the advantage that, as can be seen from equation 20 the differential gain can be simply changed by  $R_3$ .

**3.1.4** The circuit shown in Fig. 3.4 has the advantage that the gain can be linearly controlled by one resistor.

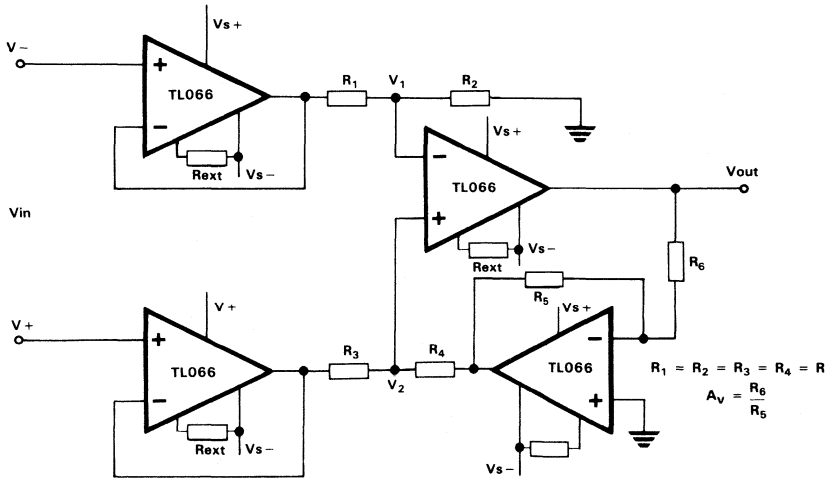


Fig. 3.4 Variable Gain Instrumentation Amplifier

$$\text{From Fig. 3.4 } V_1 = V_- \times \frac{R_2}{R_2 + R_1} \quad 21.$$

$$\text{and } V_2 = V_+ \times \frac{R_4}{R_3 + R_4} - V_{\text{out}} \times \frac{R_5}{R_6} \times \frac{R_3}{R_3 + R_4} \quad 22.$$

$$\therefore V_{\text{out}} = \frac{R_6}{R_5} \times \frac{R_3 + R_4}{R_3} \left( V_+ \times \frac{R_4}{R_3 + R_4} - V_- \times \frac{R_2}{R_2 + R_1} \right) \text{ since } V_1 = V_2 \quad 23.$$

If  $R_1 = R_2 = R_3 = R_4 = R$

$$V_{\text{out}} = \frac{R_6}{R_5} (V_+ - V_-) \quad 24.$$

Thus the gain is linearly dependant on  $R_6$  which to ensure stability should be greater or equal to  $R_5$ .

Common mode rejection

$$\text{For } R_1 = R_2 = R_3 = R = \frac{R_4}{1.1}$$

from 23 for  $V_+ = V_- = V$

$$V_{\text{out}} \approx \frac{R_6}{R_5} \times 0.05 \quad 25.$$

$$\therefore \text{CMRR} = \frac{\frac{R_6}{R_5}}{\frac{R_6}{R_5} \times 0.05} = 20 \text{ or } 26\text{dB} \quad 26.$$

Thus whilst having the advantage that the gain can be linearly set by one resistor, this circuit is subject to a high degree of CMRR degradation caused by resistor mismatches, which unlike the previous circuits is independent of differential gain.

### 3.2 Low Noise Audio Amplifier

The TL072 series of low noise BIFET op amps are eminently suitable for audio applications. They can be used for low-level low-noise applications such as pre-amplifiers or in higher level stages, such as mixers, where the high slew rate minimises the possibility of transient intermodulation distortion.

Fig 3.5 shows a circuit for a low noise magnetic cartridge pre-amp.



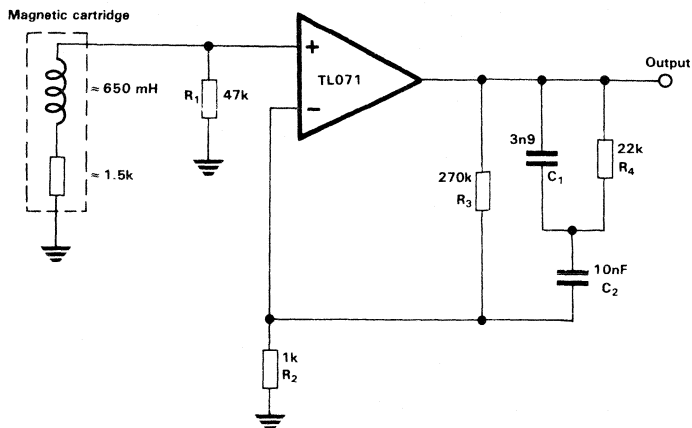


Fig. 3.5 Low Noise Magnetic Cartridge Pre-Amp

The frequency response can be evaluated from the usual formulae, which with component values *exactly* as shown gives as a result:

$$\text{T.F.} = \frac{2.32 \times 10^{-4} s^2 + 8.56 \times 10^1 s + 271 \times 10^3}{1.23 \times 10^{-11} s^3 + 2.3 \times 10^{-4} s^2 + 3.0 \times s + 10^3}$$

This is plotted along with the ideal RIAA equalisation curve, in Fig. 3.6 which shows how accurately the required response can be emulated using an

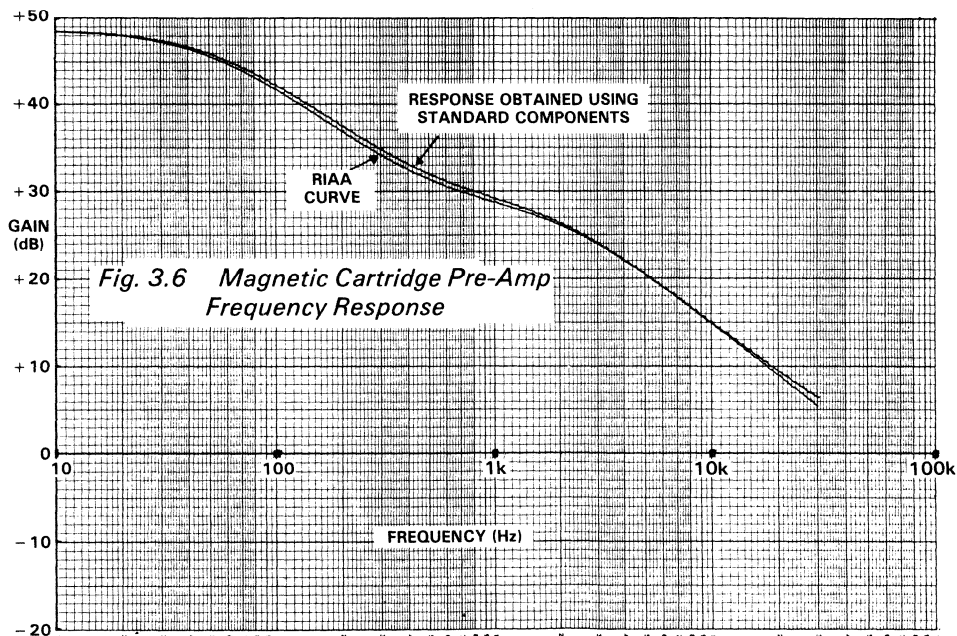


Fig. 3.6 Magnetic Cartridge Pre-Amp Frequency Response

operational amplifier. If the designer is free to use non standard components then the RIAA curve may be reproduced with extreme accuracy.

The circuit shown in Fig. 3.5 is d.c. coupled and hence the input offset voltage is multiplied by the d.c. gain of the stage, 271. This therefore requires that the following stage is a.c. coupled. This may not be considered desirable since large coupling capacitors can often cause problems on recovery from transient overloads. Consequently it is perfectly feasible to add a 100  $\mu$ F tantalum capacitor in series with  $R_2$ , which in conjunction with a low offset (– B) selection for A1, will eliminate the need to a.c. couple to the next stage.

**3.2.1 Noise Performance** Amplifier noise performances are often quoted as equivalent input noise spectral densities of both voltage and current noises i.e.  $e_n$  volts<sup>2</sup>/Hz and  $i_n$  amps<sup>2</sup>/Hz. Note that these are noise *densities* or noise voltages or currents in a bandwidth of 1Hz. It can often be assumed that  $e_n$  and  $i_n$  are constant with frequency, although in practice they seldom are and such effects will be dealt with later.

Consider initially noise voltage spectral densities,  $e_n$ ;

If the amplifier in question had a fixed gain of A independent of frequency then the noise output due to  $e_n$  would be:

$$E_n \text{ (volts r.m.s)} = \sqrt{\int_0^{\infty} e_n \times A^2 \times df}$$

which in this case would be infinite. However if the amplifier has a frequency dependent gain (as in all real systems) of  $A \times H(f)$  which has a magnitude of  $A \times |H(f)|$ , then the output noise becomes:

$$E_n \text{ (volts r.m.s)} = \sqrt{\int_0^{\infty} e_n \times A^2 \times |H(f)|^2 \times df}$$

$$\text{or } E_n = \sqrt{e_n} \times A \times \sqrt{\int_0^{\infty} |H(f)|^2 \times df}$$

The quantity  $\sqrt{e_n} \times \sqrt{\int_0^{\infty} |H(f)|^2 \times df}$  represents the equivalent wide band input noise voltage of the amplifier, since it is independent of the gain A.

The function  $\int_0^{\infty} |H(f)|^2 \times df$  is often termed the noise equivalent bandwidth (N.E.B) of the system. Correctly it should be evaluated between frequencies of 0 and  $\infty$  although in practical cases these limits can be replaced with finite frequencies.

In simple cases the N.E.B of a system may be evaluated algebraically e.g. it can be shown that the N.E.B of a single pole at  $f_b$  is equal to

$$f_b \times \frac{\pi}{2} \text{ Hz.}$$

In more complicated cases it is best to evaluate the N.E.B. numerically with the aid of a numerical integration routine.

A similar set of equations may be written for the current noise spectral density,  $i_n$ , although it is often more convenient to evaluate the effect of both noise sources in terms of a total equivalent input noise voltage in the case of a voltage amplifier or input noise current in the case of a current amplifier.

Fig.3.7 shows a model of the op amp noise contributions. From this it can be seen that the noise contributions can be summed to produce a total equivalent noise spectral density:

$$e_{nTOT} = e_n + i_{n1} \times R_1^2 + i_{n2} \times R_2^2$$

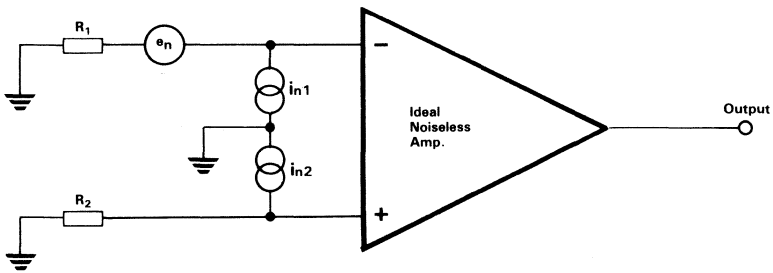


Fig. 3.7 Model of Op Amp Noise Contributions

Note that if the two source impedances are not purely resistive then the frequency response of the amplifier as seen by the noise source in question is changed. In this case the NEB for each noise source must be evaluated and the noise contribution summed at the output of the system. This technique is also applicable in cases where the noise spectral density is frequency dependent.

**3.2.2 Noise Calculations** Since the bias current of a BIFET is so small the resulting noise current is, in virtually every case, negligible. Thus the noise source in a BIFET op amp is purely a voltage noise.

The pre-amplifier transfer function given above can be re-written as:

$$TF = 271 \left[ \frac{8.56 \times 10^{-7}s^2 + 3.16 \times 10^{-1}s + 10^3}{1.23 \times 10^{-11}s^3 + 2.37 \times 10^{-4}s^2 + 3.0 \times s + 10^3} \right]$$

producing a term for A and one for H(f).

Numerical evaluation of the H(f) produces a N.E.B of 118Hz, evaluated between 1Hz and 100KHz.

∴ Equivalent wide band input noise voltage

$$\begin{aligned}
 &= \sqrt{e_n \times 118} \\
 &= \sqrt{(18\text{nV})^2 \times 118} \quad (\text{Typ value from data sheet}) \\
 &= \underline{196\text{nV}}
 \end{aligned}$$

As an example of cases with noise current sources as well, consider a device, typical of the current generation of dedicated low noise bipolar pre-amplifier having an  $e_n$  of  $1.44 \times 10^{-16}$  volts<sup>2</sup>/Hz ( $12\text{nV}/\sqrt{\text{Hz}}$ ) and  $i_n$  of  $1.69 \times 10^{-24}$  amps<sup>2</sup>/Hz ( $1.3\text{pA}/\sqrt{\text{Hz}}$ ).

The voltage noise calculation is as above however the current noise calculations are slightly more complicated.

The current noise in the inverting input sees an impedance which is dominated by the  $1\text{k}\Omega$  resistor  $R_2$  thus this is assumed to be equivalent to a voltage spectral density of  $i_n \cdot (1 \times 10^3)^2$ .

The current noise in the non-inverting terminal sees the impedance of the magnetic cartridge (the model for which is taken from data on the Shure M95 series) in parallel with the  $47\text{k}$  resistor  $R_1$ . This parallel combination results in an impedance of:

$$Z = 1.45 \times 10^3 \left[ \frac{2.1 \times 10^1\text{s} + 4.85 \times 10^4}{0.65\text{s} + 48.5 \times 10^3} \right]$$

The  $1.45 \times 10^3$  represents the equivalent d.c. resistance ( $47\text{k}$  and  $1.5\text{k}$  in parallel) whilst the terms in brackets represents a change to the effective frequency response.

Thus the N.E.B for this current noise is the N.E.B of:

$$NEB_i = \frac{8.56 \times 10^{-7}\text{s}^2 + 3.16 \times 10^{-1}\text{s} + 10^3}{1.23 \times 10^{-11}\text{s}^3 + 2.37 \times 10^{-4}\text{s}^2 + 3.0\text{s} + 10^3} \times \frac{2.1 \times 10^1\text{s} + 4.85 \times 10^4}{0.65\text{s} + 48.5 \times 10^3}$$

which was evaluated numerically between  $1\text{Hz}$  and  $100\text{kHz}$  and found to be  $6.06 \times 10^3 \text{ Hz}$ .

Thus total equivalent input noise voltage,  $E_{n\text{TOT}}$

$$\begin{aligned}
 &= \sqrt{e_n \cdot NEB_v + i_n (1 \times 10^3)^2 \cdot NEB_v + i_n (1.45 \times 10^3)^2 \cdot NEB_i} \\
 &= \sqrt{1.44 \times 10^{-16} \times 118 + 1.69 \times 10^{-24} \times 10^6 \times 118 + 1.69 \times 10^{-24} \times 2.1 \times 10^6 \times 6.06 \times 10^3} \\
 &= \sqrt{1.7 \times 10^{-14} + 2.0 \times 10^{-16} + 2.15 \times 10^{-14}} \\
 &= \sqrt{3.87 \times 10^{-14}} \\
 &= \underline{1.97 \times 10^{-7}\text{V} = 197\text{nV}}
 \end{aligned}$$

Thus a device with a seemingly lower input noise voltage has exactly the same noise performance as the BIFET amplifier with its negligible noise current. This latter feature enables the BIFET to surpass the noise performance of its bipolar equivalents especially in high impedance applications.

### 3.3 Logarithmic Amplifier

Of all the non linear elements which may be used to produce a logarithmic conversion, still the most predictable and accurate over a very wide dynamic range is the bipolar transistor. The transistor equation given below is valid over more than seven decades.

$$I_{CS} = I_0 \left[ e^{q V_{BE}/kT} - 1 \right] \quad 1.$$

where  $q$  = electronic charge

$k$  = Boltzman's constant

$I_{CS}$  = short circuit collector current

$V_{BE}$  = base-emitter voltage

$I_0$  is a constant, usually in the order of  $10^{-15}$  A for a silicon planar transistor

$T$  is absolute temperature

For  $I_{CS} \gg I_0$  equation 1 reduces to

$$I_{CS} = I_0 \cdot e^{q V_{BE}/kT} \quad 2.$$

For two transistors having collector currents  $I_{CS1}$  and  $I_{CS2}$  the ratio of the currents is given by:

$$\frac{I_{CS1}}{I_{CS2}} = \left[ e^{[q(V_{BE1} - V_{BE2})/kT]} \right] \frac{I_{01}}{I_{02}} \quad 3.$$

Thus for a closely matched pair as in a dual transistor, where  $I_{01} \approx I_{02}$

$$\text{then } \frac{I_{CS1}}{I_{CS2}} = e^{q(V_{BE1} - V_{BE2})/kT} \quad 4.$$

$$\text{or taken natural logs } (V_{BE1} - V_{BE2}) = \frac{kT}{q} \cdot \left( \log_e \frac{I_{CS1}}{I_{CS2}} \right) \quad 5.$$

The circuit shown in Fig. 3.8 was constructed as a model of equation 5.

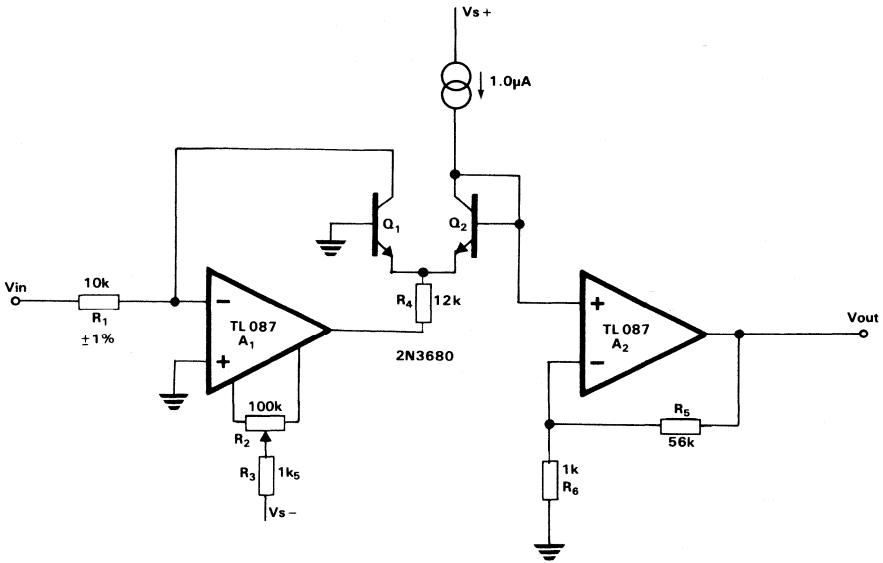


Fig. 3.8 Logarithmic Amplifier

$I_{cs_1}$  is forced by A1 to be  $\frac{V_{in}}{R_1}$

Thus from equation 5

$$V_{out} = \left( \frac{R_5}{R_6} + 1 \right) \times -\frac{kT}{q} \cdot \left( \log_e \left( \frac{V_{in}}{R_1 I_{cs_2}} \right) \right) \quad 6.$$

The  $-$  sign is a result of taking  $V_{BE2} - V_{BE1}$  rather than  $V_{BE1} - V_{BE2}$  as in equation 5.

$I_{cs_2}$  is fixed by the constant current source to be  $1\mu A$ . (It is possible to use another op amp around Q2 to establish the constant current. However this results in 2 op amps within a feedback loop and hence response speed must be sacrificed to ensure stability. The circuit in Fig. 3.8 used a transistor as the basic current source).

Thus from 6

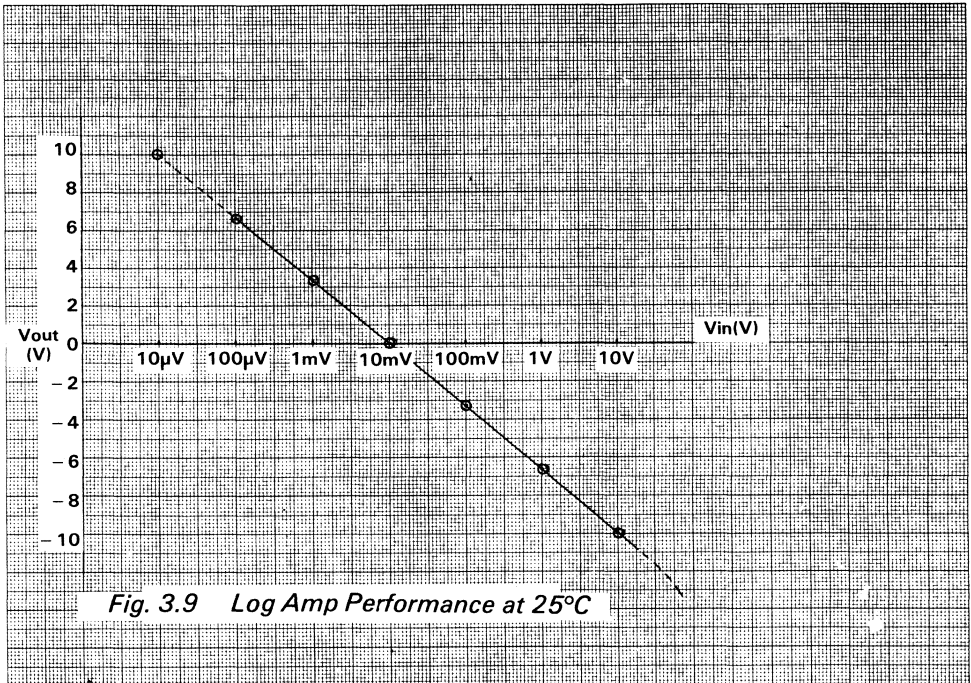
$$V_{out} = - \left( \frac{R_5}{R_6} + 1 \right) \times \frac{kT}{q} \cdot \left( \log_e(V_{in} \times 100) \right) \quad 7.$$

At  $25^\circ C$ ,  $kT/q$  equals  $25.7mV$  and this term represents a scale factor which is temperature dependent. For laboratory investigations it is possible to monitor

the temperature and hence compensate for the changing scale factor. However in practical application it is necessary to temperature compensate A2 (normally in the form of making  $R_6$  proportional to temperature) to nullify the change.

**3.3.1 Logarithmic Amplifier Performance.** Before taking any measurements, the input offset potentiometer for A1 was carefully adjusted to produce zero at the output of A1 for  $V_{in} = 0v$ . (It is essential that this potentiometer is a high resolution multi-turn type).

Fig. 3.9 shows the measured output voltage plotted against  $V_{in}$ .

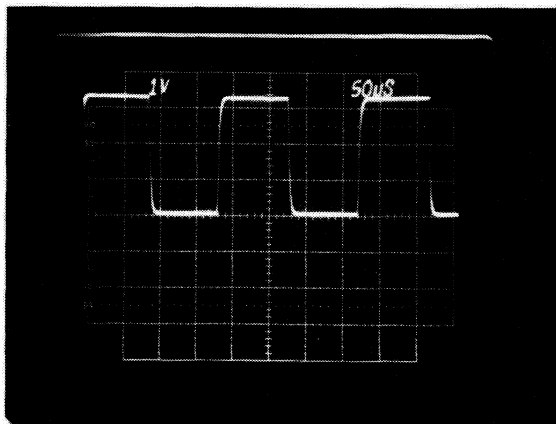


This shows the circuit to be accurate over a dynamic range of more than 100dB and also two other phenomena:

Above  $V_{in} = 20V$  (approx.) the line becomes curved. This is due to the bulk resistances in the small geometry devices which are not considered in the idealised transistor equation.

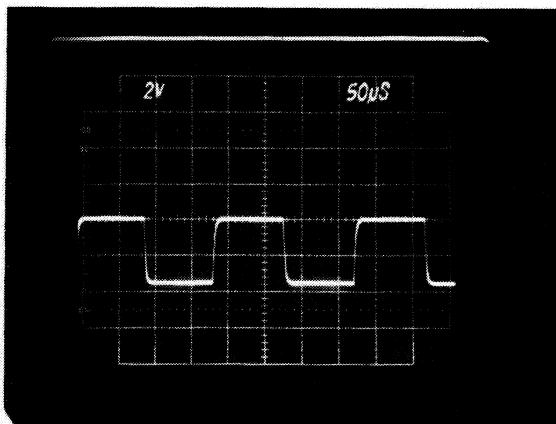
Below  $V_{in} = 100\mu V$  the performance becomes more and more difficult to monitor due to the temperature coefficient of the input offset voltage of A1. However, repeated offset adjustments allow a reading to be taken at  $V_{in} = 10\mu V$  which as can be seen falls exactly on the line. This demonstrates that the dynamic range of  $V_{out}$  against  $I_{in}$  covers more than 6 decades whilst the range of  $V_{in}$  for the circuit given in Fig. 3.8 only covers approx. 5 decades.

It is possible to increase the dynamic range of  $V_{in}$ , at the high value end, by increasing  $R_1$  since the BIFET bias currents always remain insignificant. However  $R_4$  (which is included to prevent Q1 from increasing the loop gain with consequent instability) cannot be increased or A1 output will saturate. Therefore to adopt this solution involves overcompensating A1 (a TL070A should be used) with a consequent loss of speed.



*Fig. 3.10 Output for Input 1mV – 10mV*

Figs. 3.10 to 3.13 shows photographs of the circuit outputs in response to square wave inputs between 1mV to 10mV, 10mV to 100mV, 100mV to 1V and 1V to 10V respectively. These show an approximately constant settling time of about  $8\mu\text{s}$  which is due mainly to the bandwidth limitation of A2.



*Fig. 3.11 Output for Input 10mV – 100mV*



The distortion following the  $-ve$  going edge in Fig. 3.13 is due to stray capacitance on the collector of Q2. The collector may be pulled quickly negative, due to an overshoot, but can only ramp slowly positive again with a slope of  $I_{cs}/C_{stray}$ . A better circuit layout virtually eliminated this feature.

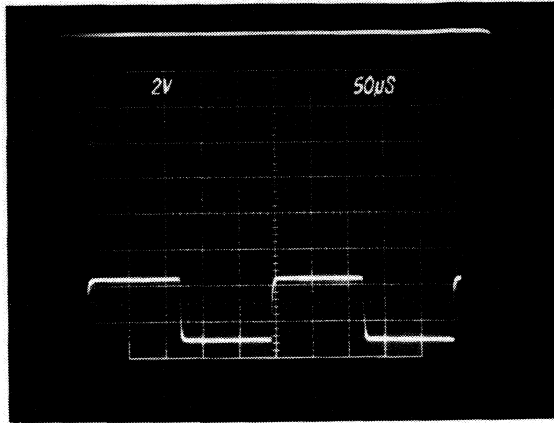


Fig 3.12 Output for Input 100mV to 1v

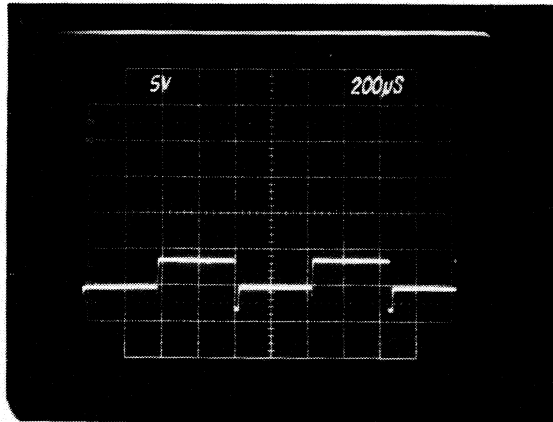


Fig. 3.13 Output for Input 1v to 10v

## 4. OSCILLATOR CIRCUITS

In this section three different oscillator circuit configurations are given. Whilst each circuit has its own advantages and disadvantages the performance of each one is enhanced by maximising the advantages of the BIFET operational amplifier.

### 4.1 Operational Amplifier Multivibrator

This is based on the classical operational amplifier multivibrator circuit as shown in Fig. 4.1. The operation of this circuit can be explained with reference to the waveforms shown in Fig. 4.2.

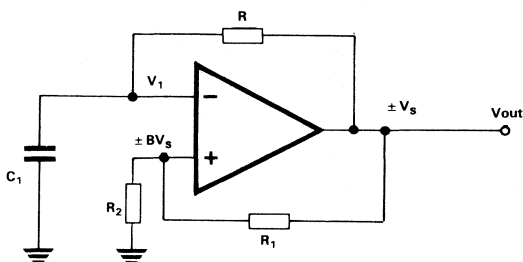


Fig. 4.1 Op Amp Multivibrator

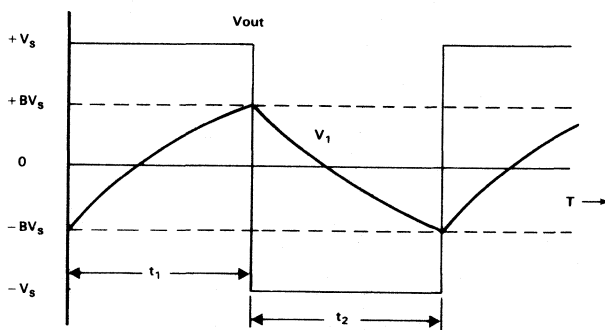


Fig. 4.2 Op Amp Multivibrator Waveforms

Assume that the op amp output can swing between  $\pm V_s$  (this may be limited by the saturation of the output stages or externally by zener diodes) and that a fraction  $B$  of this is fed back to the +ve input. The capacitor  $C_1$  charges from the op amp output via  $R$  and hence  $V_1$  increases exponentially towards  $V_s$  with a time constant  $RC_1$ . Once  $V_1$  reaches  $BV_s$  the output changes state and the procedure is repeated negatively. Thus the circuit is regenerative.

The equation describing the behaviour of  $V_1$  during time  $t_1$  is.

$$(V_s + BV_s)\left(1 - e^{-T/RC_1}\right) - BV_s = V_1 \quad 1.$$

At  $T = t_1$ ,

$$(V_s + BV_s)\left(1 - e^{-t_1/RC_1}\right) - BV_s = + BV_s \quad 2.$$

$$\therefore (1 + B) - (1 + B) e^{-t_1/RC_1} = 2B \quad 3.$$

$$\therefore \log_e \left( \frac{1 - B}{1 + B} \right) = \frac{-t_1}{RC_1} \quad 4.$$

$$\therefore t_1 = RC_1 \log_e \left( \frac{1 + B}{1 - B} \right) \quad 5.$$

$$\text{since } B = \frac{R_2}{R_1 + R_2}$$

$$t_1 = RC_1 \log_e \left( \frac{R_1 + 2R_2}{R_1} \right) \quad 6.$$

$$\text{Also since } t_1 = t_2, \text{ oscillator period} = 2RC_1 \log_e \left( \frac{R_1 + 2R_2}{R_1} \right)$$

One advantage of this circuit is that the oscillation period is independent of  $V_s$  and hence supply rail fluctuations. The most convenient method of changing the frequency is by changing either  $R$  or  $C_1$  since the period is linearly dependent upon both of these.

The performance limitations of this circuit are caused by: at high frequency - the response time of the op amp (actually functioning as a comparator) and at low frequencies the input bias current since this effects the charging rate of  $C_1$ .

A variation of this circuit, which also illustrates how a BIFET amplifier may be used to minimise the performance degradation mentioned above, is shown in Fig. 4.3

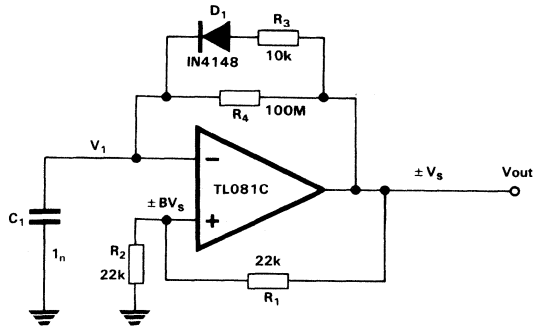


Fig. 4.3 Unequal Mark-Space Multivibrator

The only change from Fig. 4.1 is the inclusion of  $D_1$  and  $R_3$ , the effect of which is to make  $R$  (in Fig. 4.1) equal to  $R_4$  when  $V_{out} = -V_s$  and approximately equal to  $R_3$  and  $R_4$  in parallel when  $V_{out} = +V_s$ . Since in Fig. 4.3  $R_4 \gg R_3$ ,  $R$  may be considered to be equal to either  $R_3$  or  $R_4$  depending upon the polarity of  $V_{out}$ .

Equation 6 above now becomes:

$$t_1 = R_3 C_1 \log_e \left( \frac{R_1 + 2R_2}{R_1} \right)$$

and 
$$t_2 = R_4 C_1 \log_e \left( \frac{R_1 + 2R_2}{R_1} \right)$$

For the values shown in Fig. 4.3,  $t_1 \approx 10\mu s$ ,  $t_2 \approx 0.1s$  giving a mark space ratio of 1:10,000. Such an extreme value is only possible by the use of the BIFET op amp since its response time is still negligible in comparison with  $t_1$  due to its high, 13V/  $\mu s$  slew rate; whilst the input bias current has a negligible effect on  $V_1$  even when being supplied via  $R_4$ .

In general the use of a BIFET in such a circuit allows waveforms to be generated with extremely high accuracy and stability, having periods from tens of microseconds, with capacitors in the nf region, up to several minutes with capacitors of approximately  $1\mu f$  thus avoiding the use of expensive, bulky and comparatively unreliable electrolytics. If longer periods are required then they can, of course, be obtained using larger value capacitors; although tantalum types are recommended as the leakage in terms of capacity  $\times$  leakage current = constant tends to become the limiting factor.

## 4.2 Triangle Wave Generator

Once again this is a fairly well known circuit which is in a way, a development of the first circuit. It differs in that it is capable of producing triangle waves as well

as square waves by virtue of the operational amplifier integrator which replaces the simple  $RC_1$  network of Fig. 4.1. The circuit is shown in Fig. 4.4.

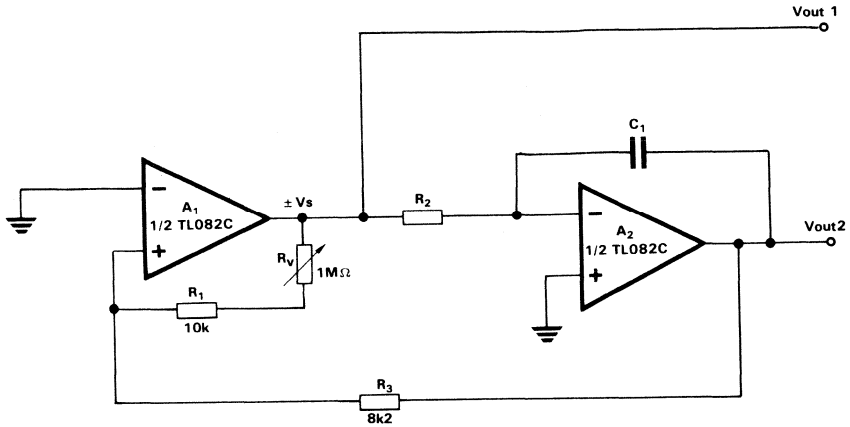


Fig. 4.4 Triangle Wave Generator

Since the integrator formed by A2 produces a sign inversion then the output ( $V_{out2}$ ) is fed back to the +ve input of A1 unlike the previous circuit. The circuit operation is very similar to before and is illustrated in Fig. 4.5

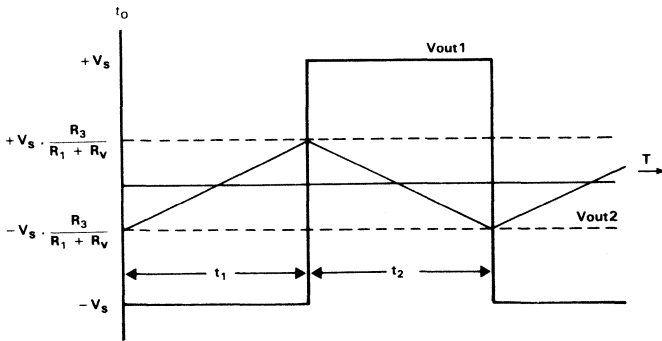


Fig. 4.5 Triangle Wave Generator Waveforms

A1 operates as a comparator and has switching thresholds

of  $\pm Vs \cdot \frac{R_3}{R_1 + R_V}$  where  $\pm Vs$  once again represents the output swing of the operational amplifier.

$$\text{Assume at } T = 0, V_{\text{out}2} = -V_s \cdot \frac{R_3}{R_1 + R_v} \quad 1.$$

$$\therefore \text{Current into integrator, } I = \frac{-V_s}{R_2} \quad 2.$$

$$\therefore \text{Integrator output} = - \frac{1}{C_1} \int_{t_0}^T I \, dt = V_{\text{out}2}(t_0) - \frac{I}{C_1} (T - t_0) \quad 3.$$

$$= V_{\text{out}2}(t_0) + \frac{V_s}{C_1 \times R_2} (T - t_0) \quad 4.$$

$$= \frac{-V_s \times R_3}{R_1 + R_v} + \frac{V_s}{C_1 \times R_2} (T - t_0) \quad 5.$$

$$\therefore \text{When } (T - t_0) = t_1: \frac{V_s \times R_3}{R_1 + R_v} = \frac{-V_s \times R_3}{R_1 + R_v} + \frac{V_s \times t_1}{C_1 \times R_2} \quad 6.$$

$$\therefore t_1 = \frac{2R_3}{R_1 + R_v} \times C_1 \times R_2 \quad 7.$$

Total period =  $t_1 + t_2$  and hence

$$f_{\text{osc}} = \frac{R_1 + R_v}{4 \times R_3 \times R_2 \times C_1} \text{ Hz} \quad 8.$$

and  $V_{\text{out}2}$  has a peak to peak value of

$$\frac{2 \times R_3 \times V_s}{R_1 + R_v} \quad 9.$$

Thus this circuit may be used to generate square waves, whose frequency may be most conveniently altered by  $C_1$  or  $R_2$ , and triangle waves of an equal frequency whose amplitude may be varied by  $R_v$ .

Using a dual BIFET maximises the versatility of this circuit and, by virtue of its high speed and low bias current, allows the frequency to be programmed over a 6 decade range by  $R_2$  if  $C_1$  has the optimal value of approximately 10nf.

### 4.3 Variable Amplitude Triangle Wave Generator

One disadvantage of the circuit shown in Fig. 4.4 is that an attempt to vary the amplitude of the triangular wave by adjusting  $R_v$  will also result in a change in frequency according to equation 8 above. In many cases this is not desirable

and the circuit shown in Fig. 4.6 was developed as a means of overcoming this limitation.

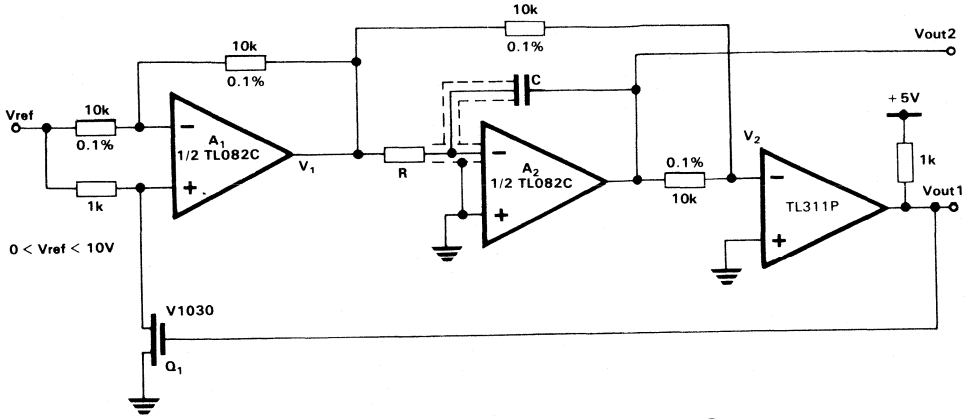


Fig. 4.6 Variable Amplitude Triangle Wave Generator

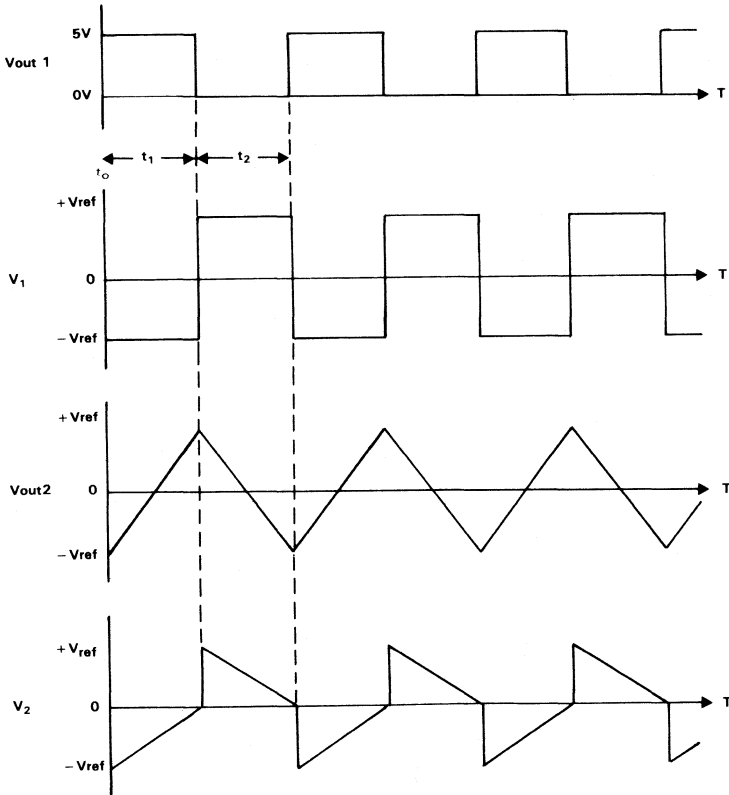


Fig. 4.7 Waveform Diagram

The circuit operation can be explained with the waveforms shown in Fig. 4.7. Amplifier A1 is configured to be either a unity gain inverting amplifier or a unity gain non-inverting amplifier, depending on whether Q1 is on or off respectively. (Q1 is one of Texas Instruments SILECT range of VMOS transistors and is used in this application for its low ON-resistance, high switching speed and above all for its extreme ease of interfacing. The V1030 is a 30v version of the 1A, 625mW series which also includes 40, 60 and 80v versions.) A2 is an integrator whose output is summed with the output of A1 and compared to zero by the TL311P comparator. (This is a direct replacement for the LM311 with the advantage of JFET input transistors).

The open collector output of the comparator has a  $1k\Omega$  pull up resistor to make it TTL compatible and also directly drives the gate of Q1. Assume the initial conditions at  $T = t_0$  as shown in Fig 4.7

i.e.  $V_{out1} = 5V$ ,  $V_{out2} = -V_{ref}$ ,  $V_2 = -V_{ref}$

Since if  $V_{out1} = 5v$ ,  $Q_1$  is ON and  $A_1$  has a gain of  $-1$ .

Hence  $V_1 = -V_{ref}$

$$\begin{aligned} \therefore \text{Output of } A_2 &= \frac{-1}{RC} \int_{t_0}^T V_1 dt \\ &= V_1(t=0) + \frac{V_{ref}}{RC} (T - t_0) \\ &= -V_{ref} + \frac{V_{ref}}{RC} (T - t_0) \end{aligned}$$

For the comparator to switch at time  $T = t_1$ ,  $V_2$  must be  $0V$  and hence  $V_{out2}$  must equal  $-V_1$

$$\therefore -V_1 = -V_{ref} + \frac{V_{ref}}{RC} \times t_1$$

but  $V_1 = -V_{ref}$

$$\therefore 2V_{ref} = \frac{V_{ref} \times t_1}{RC}$$

$$\therefore t_1 = 2RC$$

Since  $t_1 = t_2$ , total period =  $4RC$ .

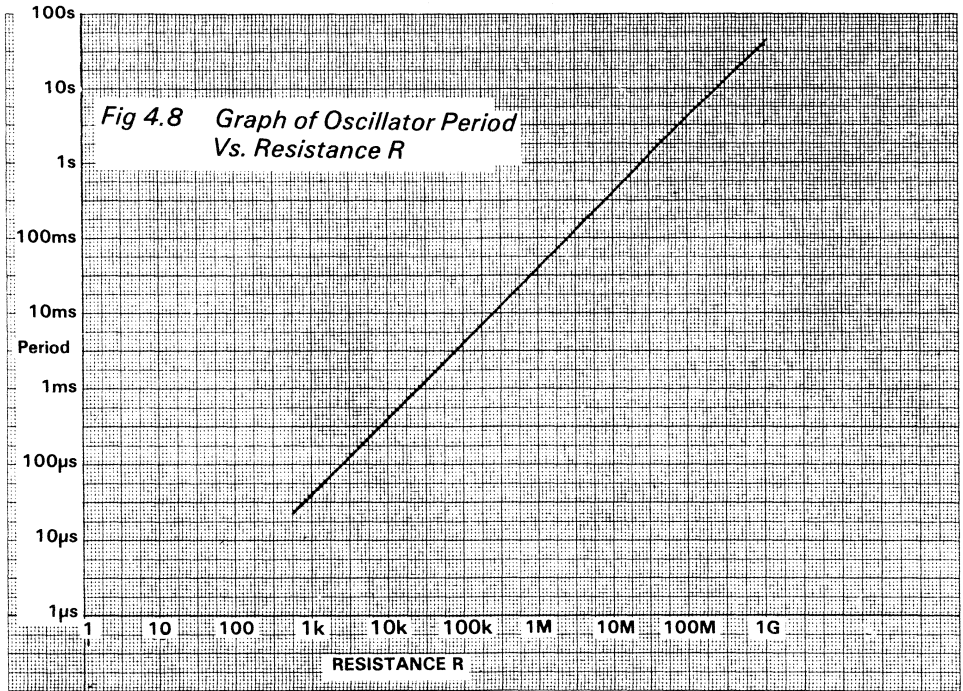
Thus the total period of the oscillation remains constant at  $4RC$  whilst the peak amplitude of the triangle wave is always preset to  $V_{ref}$ .

The high frequency performance of this oscillator is limited by the response time of the comparator, VMOS switch and amplifier A1. Thanks to the high speed of



the VMOS switch and the high slew rate of A1 this delay is reduced to the order of microseconds. The low frequency performance is limited mainly by stray leakage currents flowing into the inverting input of A2. Since R may be in  $1\text{G}\Omega$  region without encountering significant errors due to amplifier bias currents, particular attention must be paid to minimising circuit board and capacitor leakages. For this reason a guard ring, as shown in Fig. 4.6, and a polystyrene or preferably teflon capacitor are recommended.

Some experimental results are plotted in Fig. 4.8, showing that with a  $10\text{nf}$  polystyrene capacitor at  $25^\circ\text{C}$  the oscillator period was linearly dependent upon R over a more than 6 decade range.



## 5. SAMPLING CIRCUITS

Sample and hold circuits constitute one of the most useful analogue building blocks available to the linear systems designer as well as being one of the main areas where circuit performance may be greatly enhanced by the use of BIFET operational amplifiers.

### 5.1 Basic Sample and Hold

Fig 5.1 shows what is perhaps the simplest sample and hold circuit.

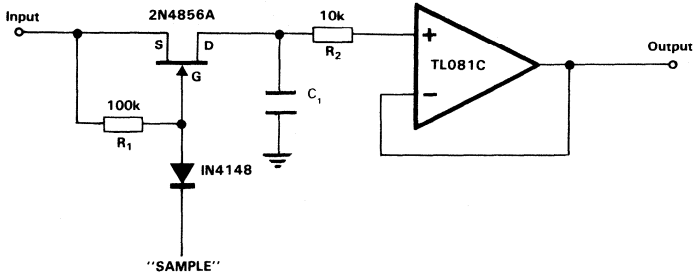


Fig. 5.1 Basic Sample and Hold Circuit

When the sample line is taken high (greater than  $V_{in}$ ) the FET turns on and the input voltage is applied to  $C_1$ . If the sample line is then taken low, pulling the gate of the FET below its pinch-off voltage, the FET turns off. Since now only leakage and bias currents can effect the state of charge of  $C_1$ , and since both are exceedingly small, the sampled input voltage is held on  $C_1$ .

The 10k resistor  $R_2$  does not effect the normal operation of the circuit in any way. Its only purpose is to protect the input stage of the op amp as this may become a discharge path for  $C_1$  should the op amp supplies suddenly disappear – FET input stages are, in fact, quite resistant to this form of damage although the inclusion of  $R_2$  is good design practice and is recommended with any op amp where the input is directly connected to a capacitor of  $1\mu f$  or greater.

#### Drift in hold mode (figures at 25°C)

Op amp bias current = 200pA max. (30pA typ.)

FET leakage current = 250pA max.

∴ Total leakage current (worst case) = 450pA

$$\text{Drift rate} = \frac{dV}{dt} = \frac{I}{C} = \frac{450 \times 10^{-12}}{C}$$

$$\begin{aligned} \text{For } C = 1\mu f, \frac{dV}{dt} &= 450 \times 10^{-6} \text{ V/sec} \\ &= \underline{\underline{0.45\text{mV/sec}}} \end{aligned}$$

To achieve drift rates of this order, it is necessary that leakage in the storage capacitor itself does not become significant. Consequently, types with low dielectric losses such as polystyrene or preferably teflon are recommended.

The time taken for the voltage on the capacitor to reach the input voltage once the sample line goes high depends on the time constant,  $\tau = R_{ds(on)} \times C_1$ . After a delay of  $5\tau$  the capacitor voltage will be within 1% of  $V_{in}$  and within .1% in  $7\tau$ .

$$\begin{aligned} \text{For } 2N4856A, R_{ds(on)} &= 25\Omega \text{ max at } V_{ds} = 0_v \\ &= 37.5\Omega \text{ max at } I_D = 20\text{mA} \end{aligned}$$

For  $C_1 = 1\mu\text{f}$ ,  $5\tau \approx 0.125\text{ms}$  (for small input changes)

The value of  $C_1$  must be chosen as a compromise between the drift during the hold mode and the time taken for the output to settle within a given percentage error of the input (once the sample command has been given) known as the acquisition time.

Since BIFET op amps have bias currents which are several orders of magnitude less than standard bipolar op amps then to achieve a given drift rate the hold capacitor may similarly be several orders of magnitude less in value, with a corresponding decrease in acquisition time.

Conversely, if the acquisition time is adequate with a given value capacitor, then changing from one of the standard bipolar op amps to a BIFET device will decrease the drift rate dramatically.

## 5.2 Low Drift Sample and Hold

The circuit shown in Fig. 5.2 is a development of that shown in Fig. 5.1 in which the leakage current through the FET switch has been effectively eliminated.

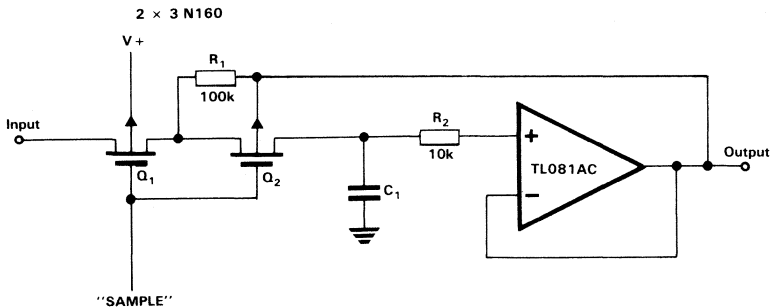


Fig. 5.2 Low Drift Sample and Hold

The FET's used as switches are P-channel enhancement types which are off for zero gate-source voltage. To turn on and hence sample the input voltage the gate must be pulled negative.

During the hold mode leakage through  $Q_1$  is absorbed by  $R_1$ .

Since even at  $125^\circ\text{C}$  leakage through  $Q_1 \leq 100\text{nA}$

$$\therefore \text{Voltage drop across } R_1 = 100 \times 10^{-9} \times 10^5\text{V} \\ = 10^{-2}\text{V} = 10\text{mV}$$

Thus maximum voltage across  $Q_2$  in hold mode =  $10\text{mV} + \text{offset voltage}$   
 $= 10\text{mV} + 7.5\text{mV} = 17.5\text{mV max @ } 70^\circ\text{C}$

This results in a reduction in the leakage current through  $Q_2$  by at least two orders of magnitude to a level which is insignificant even compared to the BIFET bias current.

$$\text{Thus drift in hold mode} = \frac{I}{C} \text{ volts/sec} = \frac{200 \times 10^{-12}}{C_1} \text{ volts/sec}$$

If  $C_1 = 1\mu\text{f}$  then drift =  $200 \times 10^{-6} = 0.2\text{mV/sec max @ } 25^\circ\text{C}$

Reverse biased silicon semiconductor leakage currents (which is what a BIFET input bias current actually is) double for every  $10^\circ\text{C}$  increase in temperature (approximately) which corresponds to a maximum drift rate of  $4.5\text{mV/sec}$  at  $70^\circ\text{C}$  although the typical drift would be at least by a factor of 6 less than this.

Note that this circuit will only work as intended provided enhancement mode MOSFETS are used for  $Q_1$  and  $Q_2$ . Any depletion device, such as a JFET, requires a negative bias to turn it off and hence  $Q_2$  once again contributes to the leakage current flowing from  $C_1$ . One disadvantage of this circuit is that since the on-resistance of MOSFETs is comparatively high (around  $200\Omega$ ) and they are effectively in series, the acquisition time is correspondingly longer.

### 5.3 High Accuracy Sample Hold

The previous two sample and hold circuits have both been open loop systems where errors due offsets etc. have been allowed to accumulate along the system. The circuit shown in Fig 5.3 is a closed loop system where in the

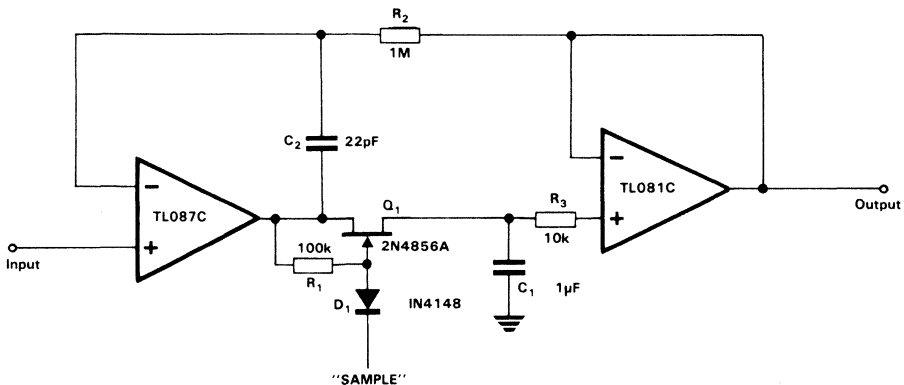


Fig. 5.3 High Accuracy Sample and Hold

sampling state, after a fixed settling time, the output and input differ only by the offset voltage of A1 since A2 is within the closed loop and its offset voltage is of no consequence.

Thus a TL087C may be used for A1 giving a max offset voltage of 0.5mV at 25°C whilst A2 can be a TL081C.

Components  $R_2$  and  $C_2$  guarantee loop stability during the sampling mode and compensate for the open loop pole generated by  $R_{ds}(on)$  and  $C_1$ .

During the hold mode with Q1 off A1 goes "open loop" and its output will almost certainly saturate. This may or may not cause a problem depending upon the drive level applied to the FET gate, but possible solutions to either externally limit the output swing of A1 or place a second FET in parallel with  $C_2$ , driven in antiphase with Q1 such that A1 does not go open loop.

Drift rate calculations are as for the first sample and hold circuit as is the estimation of acquisition time provided that  $R_2 \times C_2 = R_{ds}(on) \times C_1$  (also a condition for loop stability).

### 5.4 Peak Detector

A peak detector is, in essence, a sample and hold circuit used in conjunction with a comparator. A simple circuit is given in Fig. 5.4.

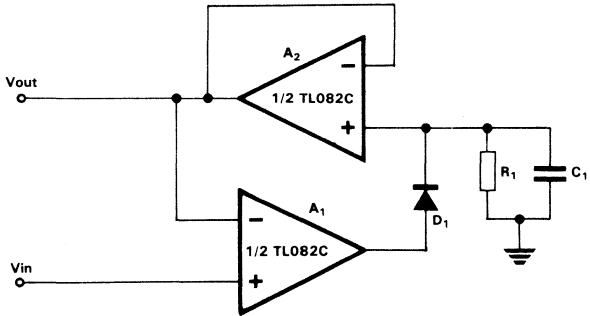


Fig. 5.4 Simple Peak Detector

If  $V_{in}$  is greater than  $V_{out}$ , the output of A1 goes +ve increasing the voltage on  $C_1$  until  $V_{out} = V_{in}$ . When  $V_{in}$  later falls below  $V_{out}$ , A1 output goes negative, reverse biasing D1 leaving the voltage on  $C_1$  (and hence  $V_{out}$ ) to decay away with a time constant of  $R_1 C_1$ .

The main requirement for the op amps used in this circuit is high bandwidth and slew rate since A1 output must respond extremely quickly to react to fast peak transients on the input.

An obvious application for such a circuit is in an audio peak power meter where the output of the circuit shown in Fig. 5.4 would be fed to an LED bar graph driver or simple analogue panel meter to indicate the peak programme power content.

### 5.5 Low Drift Peak Detector

Fig. 5.5 shows a development of the simple peak detector in which the performance in terms of speed and drift have been improved.

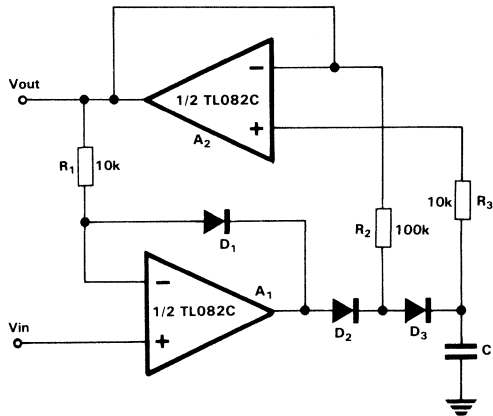


Fig. 5.5 Low Drift Peak Detector

During peaks the circuit operates as before,  $C_1$  being charged from A1 output until  $V_{out} = V_{in}$ . Once  $V_{out}$  exceeds  $V_{in}$ , A1 output goes negative but is prevented from saturating by D1 and hence the response time for the next input transient is improved. D2 and D3 function in a similar manner to the two FETs in the low drift sample and hold circuit.  $R_2$  absorbs the leakage from D2 whilst D3 completely isolates  $C_1$ . Drift calculations are exactly as for the low drift sample and hold circuit.

## 6. FILTER CIRCUITS

This section gives the description and analysis of a number of useful filter circuits which may be constructed with BIFET op amps.

### 6.1 The Integrator

The integrator is perhaps the most common and useful frequency sensitive network or analogue computer component available. It's basic form is shown in Fig. 6.1.

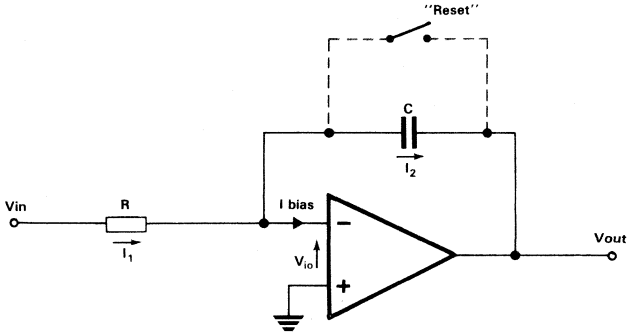


Fig. 6.1 The Integrator

If  $I_{bias} = 0$ ,  $V_{io} = 0$  and the amplifier gain is infinite then  $I_1 = I_2$ .

$$\therefore \frac{V_{in}}{R} = \frac{-dV_{out}}{dt} \times C$$

Integrating both sides,

$$V_{out} = \frac{-1}{RC} \int_{t_1}^{t_2} V_{in}.dt + C$$

where C is the constant of integration and corresponds to the initial conditions.

Thus an integrator is formed with a scale factor of  $-\frac{1}{RC}$ . The initial conditions must be set up prior to any required integration. This is often performed using some form of reset switch – shown dotted in the diagram.

The effect of the offset voltage  $V_{io}$  is to effectively alter the input voltage by that amount. This is seldom significant except when  $V_{in} \approx 0V$ . If  $I_1 = 0$  (input open circuit) then  $I_2 = -I_{bias}$ . This gives rise to a ramp at the output having a slope  $I_{bias}/C$  (Volts/sec). Since for BIFET op amps  $I_{bias}$  is extremely small, this output ramp can usually be neglected unless very small values of C are used.

Taking the Laplace transform of the integrator transfer function,

$$V_{out} = \frac{-1}{R \times C \times s} \times V_{in}$$

which will be used in the analysis of the first filter circuit.

## 6.2 The State Variable Filter

The state variable filter is simply a filter in which integrators have been used to construct an analogue computer model of the basic filter transfer function.

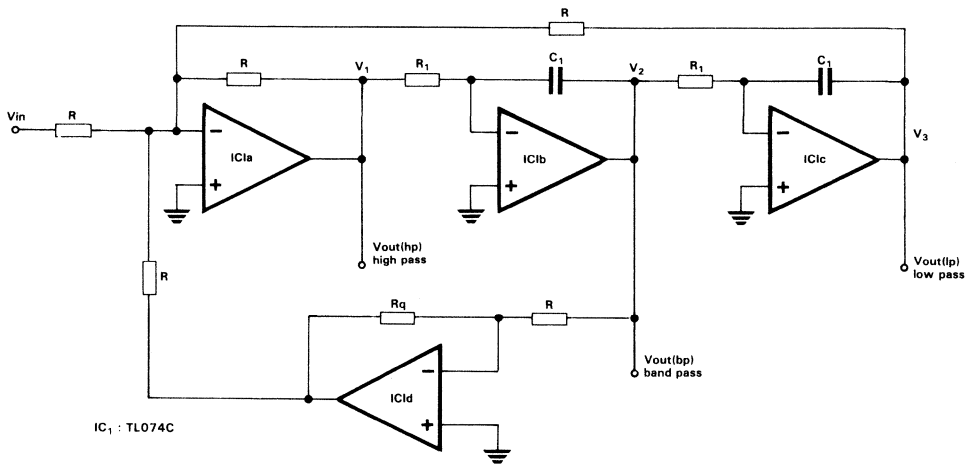


Fig. 6.2 Second Order State Variable Filter

Fig. 6.2 shows the circuit of the basic second-order filter, from which

$$V_1 = - \left( V_{in} - V_2 \times \frac{R_q}{R} + V_3 \right) \quad 1.$$

$$V_2 = - \frac{1}{R_1 C_1 \times s} \times V_1 \quad 2.$$

$$V_3 = - \frac{1}{R_1 C_1 \times s} \times V_2 = \frac{1}{(R_1 \times C_1)^2 s^2} V_1 \quad 3.$$

These three equations completely define the circuit behaviour.



Re-arranging gives:

$$V_1 = - \left( V_{in} + \frac{1}{R_1 \times C_1 \times s} \times V_1 \times \frac{R_q}{R} + \frac{1}{(R_1 C_1)^2 s^2} V_1 \right) \quad 4.$$

$$\therefore V_1 = \frac{-V_{in} s^2}{s^2 + \frac{1}{R_1 C_1} \times s \times \frac{R_q}{R} + \frac{1}{(R_1 C_1)^2}} \quad 5.$$

Writing 1 in terms of  $V_{in}$  and  $V_2$

$$s.V_2.R_1.C_1 = \left( V_{in} - V_2 \frac{R_q}{R} - \frac{V_2}{R_1 C_1 s} \right) \quad 6.$$

$$\therefore V_2 = \frac{V_{in} \times \frac{1}{R_1 C_1} \times s}{s^2 + \frac{1}{R_1 C_1} \times s \times \frac{R_q}{R} + \frac{1}{(R_1 C_1)^2}} \quad 7.$$

Writing 3 in terms of  $V_{in}$  and  $V_3$

$$V_3.s^2.(R_1 C_1)^2 = - \left( V_{in} + V_3.s R_1 C_1 \frac{R_q}{R} + V_3 \right) \quad 8.$$

$$\therefore V_3 = \frac{-V_{in} \times \frac{1}{(R_1 C_1)^2}}{s^2 + \frac{1}{R_1 C_1} \times s \times \frac{R_q}{R} + \frac{1}{(R_1 C_1)^2}} \quad 9.$$

Comparing 5, 7 and 9 with the standard forms for high pass, bandpass and low pass filters respectively;

High Pass:

$$\therefore V_{out} (hp) = \frac{V_{in} \times s^2}{s^2 + \frac{\omega_0}{Q} \times s + \omega_0^2}$$

Band Pass:

$$\therefore V_{out} (bp) = \frac{V_{in} \times s \times \omega_0}{s^2 + \frac{s \omega_0}{Q} + \omega_0^2}$$

Low Pass:

$$\therefore V_{out} (Ip) = \frac{\omega_0^2}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}$$

it is clear that all three types of filters, high pass, band pass and low pass are available simultaneously from  $V_1$ ,  $V_2$  and  $V_3$  respectively and that in each case

$$Q = \frac{R}{R_q} \text{ and } \omega_0 = \frac{1}{R_1 C_1}$$

As a general purpose filter block the state variable filter is extremely useful since  $Q$  may be varied using  $R_q$  and  $\omega_0$  by changing either  $C_1$  or  $R_1$ .

The TL074C quad BIFET is ideally suited to this application because of its low noise, high bandwidth and slew rate and since only one package is required. The very small bias currents means that very high values of  $R_1$  can be used (in excess of  $10M\Omega$  if required) and hence for a given  $\omega_0$ ,  $C_1$  can be quite small. This is extremely advantageous since it is far easier to get an inexpensive physically small and temperature stable small value capacitor than it is a large one. Thus it is quite viable to produce a filter with an  $\omega_0$  of 64.4 rads/sec ( $\approx 10\text{Hz}$ ) and a  $Q$  of 5 using  $R=10k$ ,  $R_q=2k$ ,  $R_1=3M3$  and  $C_1$  of only 4.7nf.

### 6.3 Sallen-Key Filters

Although the state-variable is an excellent general purpose filter it is not really suitable for use in production as it is comparatively wasteful of op amps. In many applications, particularly those with a low  $Q$  ( $< 1.5$ ) the Sallen-key filter\* shown in Fig. 6.3 is more suitable.

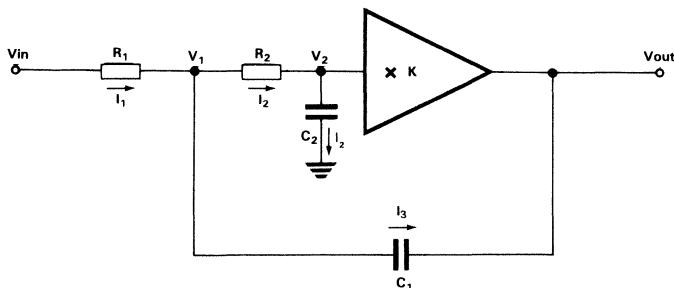


Fig. 6.3 Second-Order Low Pass Sallen-Key Filter

\*Sallen, P.R.; Key, E.L.: a practical method of designing RC active filters. IRE Trans. CT – 2(1955), pp 74–85.

From Fig. 6.3

$$I_1 = \frac{V_{in} - V_1}{R_1} = I_2 + I_3 = \frac{V_1 - V_2}{R_2} + (V_1 - KV_2) sC_1 \quad 1.$$

$$\text{and } V_1 = V_2(1 + R_2C_2s) \quad 2.$$

$$\therefore V_{in} = [(1 + R_2C_2s) + R_1C_2s + (R_2C_2s + (1 - K)) sC_1R_1] V_2 \quad 3.$$

$$\therefore V_{in} = V_2[1 + s(R_2C_2 + R_1C_2 + (1 - K)R_1C_1) + s^2C_1C_2R_1R_2] \quad 4.$$

$$\therefore \frac{V_{out}}{V_{in}} = \frac{KV_2}{V_{in}} = \frac{K}{1 + s(R_2C_2 + R_1C_2 + (1 - K)R_1C_1) + s^2C_1C_2R_1R_2} \quad 5.$$

$$\therefore \frac{V_{out}}{V_{in}} = \frac{1}{R_1R_2C_1C_2} \times \frac{K}{s^2 + \left[ \frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1 - K}{R_2C_2} \right] s + \frac{1}{R_1R_2C_1C_2}} \quad 6.$$

Before designing a filter from this equation it is wise to make some simplifying assumptions. These are very much a matter of personal preference since all are as equally valid as the three given below.

a) Let  $R_1 = R_2 = R$ ,  $K = 1$

$$\therefore \frac{V_{out}}{V_{in}} = \frac{1}{R^2C_1C_2} \times \frac{1}{s^2 + \frac{2}{RC_1} s + \frac{1}{R^2C_1C_2}}$$

$$\text{hence } \omega_0 = \frac{1}{R\sqrt{C_1C_2}} \text{ and } Q = \frac{\sqrt{C_1/C_2}}{2}$$

b) Let  $C_1 = C_2 = C$ ,  $K = 1$

$$\therefore \frac{V_{out}}{V_{in}} = \frac{1}{R_1R_2C^2} \times \frac{1}{s^2 + \left[ \frac{1}{R_1C} + \frac{1}{R_2C} \right] s + \frac{1}{R_1R_2C^2}}$$

$$\text{hence } \omega_0 = \frac{1}{C\sqrt{R_1 \times R_2}} \text{ and } Q = \frac{\sqrt{R_1 \times R_2}}{R_1 + R_2}$$

c) Let  $R_2 = \alpha R_1$ ,  $C_2 = \frac{C_1}{\alpha}$ ,  $K = 1$

$$\therefore \frac{V_{out}}{V_{in}} = \frac{1}{R_1^2 C_1^2} \times \frac{1}{s^2 + \left[ \frac{1}{\alpha R_1 \times C_2} + \frac{1}{R_1 C_1} \right] s + \frac{1}{R_1^2 \times C_1^2}}$$

$$\therefore \omega_0 = \frac{1}{R_1 C_1} \text{ and } Q = \frac{\alpha}{1 + \alpha}$$

d)  $R_1 = R_2 = R$ ,  $C_1 = C_2 = C$  (equal component value case)

$$\therefore \frac{V_{out}}{V_{in}} = \frac{1}{R^2 C^2} \times \frac{K}{s^2 + \frac{(3-K)}{R \times C} \times s + \frac{1}{R^2 C^2}}$$

$$\therefore \omega_0 = \frac{1}{RC} \text{ and } Q = \frac{1}{3-K}$$

Cases a), b) and c) are known as unity gain Sallen-Key filters and have two main drawbacks. First  $\omega_0$  and  $Q$  are always interdependent. The interdependence in cases a) and b) are quite complex and involve a complete redesign for any parameter change. Case c) attempts to clarify the interrelationship by assuming  $R_1 C_1 = R_2 C_2$  but even this cannot remove the interdependence.

Case d) is slightly different and is known as the equal component value (ECV) Sallen-Key filter. It results in the circuit shown in Fig. 6.4. For this case  $Q$  may be adjusted by varying one resistor without effecting  $\omega_0$ .

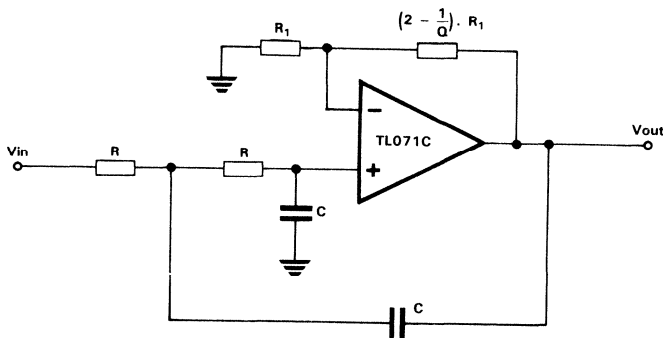
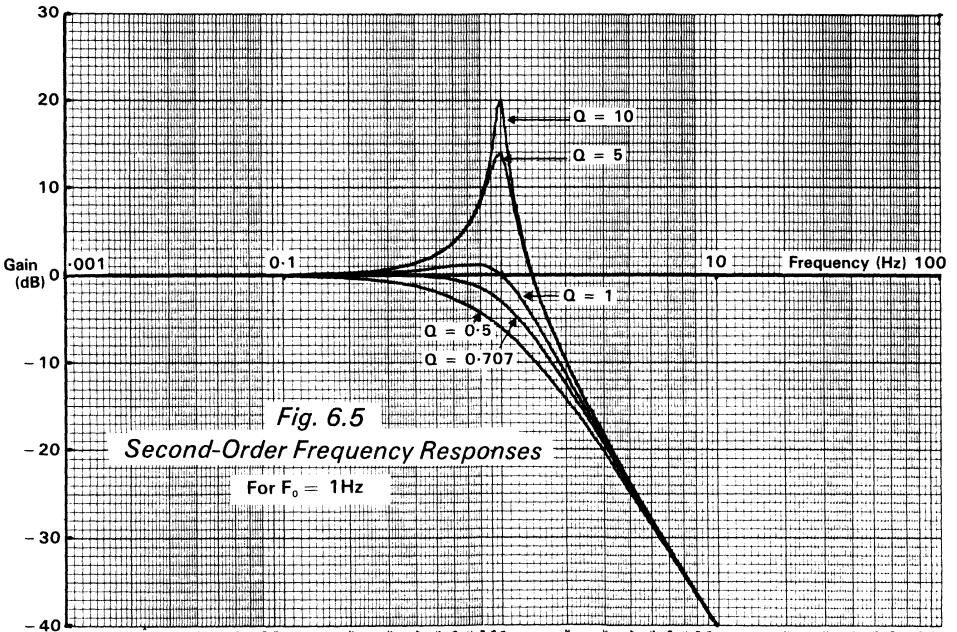


Fig. 6.4 Equal Component Value (ECV) Sallen-Key Filter

Given below are a number of notes relating to the Sallen-Key filter and active filters in general.

- 1) Accurate temperature stable capacitors are always more easily available in small values (also less expensive and physically smaller). Hence for low  $\omega_0$  scale Rs rather than Cs (Errors due to BIFET bias currents usually negligible).
- 2) Ensure that the op amp has a gain-bandwidth of 5 to 10 times the filter gain-frequency product at resonance. Also ensure that the op amp power bandwidth (frequency above which op amp produces distortion at max. output swing due to slew rate limiting) is adequate (741 type op amps only have a power bandwidth of 10kHz).
- 3) In Sallen-Key filters a low pass response may be converted into the equivalent high pass merely by transposing Rs and Cs on the circuit diagram.
- 4) When designing very high Q filters (>50) it is always better to obtain this response by cascading lower Q filters since a single high Q stage is very sensitive to component mismatches and spurious oscillation may result.
- 5) As a guide to the selection of the appropriate response for a particular application a number of low pass second order frequency responses are shown in Fig. 6.5, all normalised to  $F_0 = 1\text{Hz}$ . The corresponding responses to a unity step input are shown in Fig. 6.6.



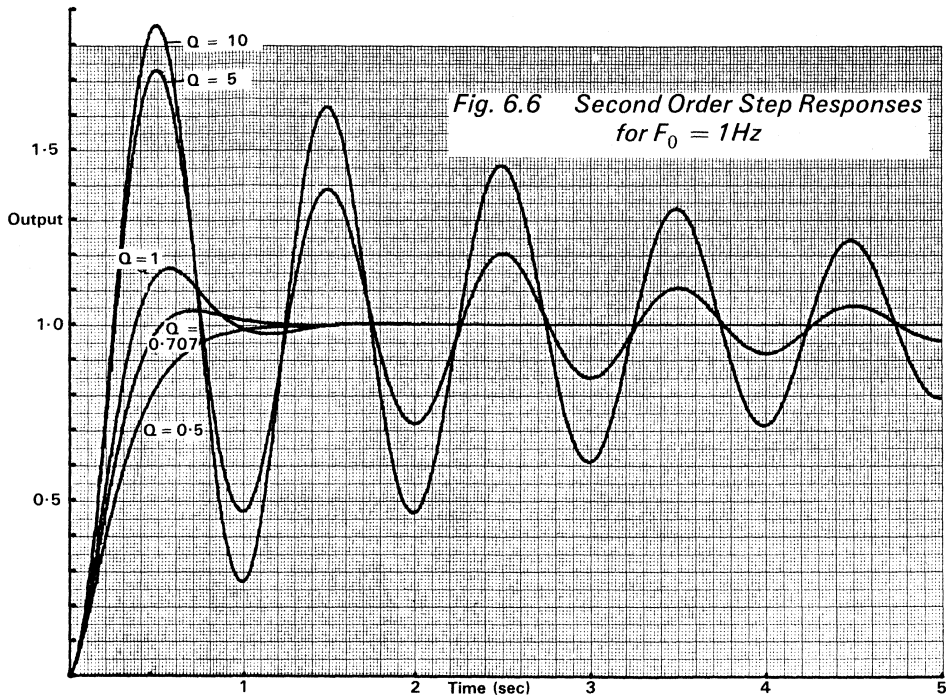


Fig. 6.6 Second Order Step Responses for  $F_0 = 1\text{Hz}$

### 6.4 "Twin T" Notch Filter

The "twin T" filter is extremely useful in that it is one of the few RC filters which produce (in theory at least) an infinitely deep notch. Its standard form is shown in Fig. 6.7 where the components have been chosen to produce a notch at approximately 50Hz. The use of the BIFET buffer in this case allows the impedance level to be relatively high to avoid the use of large value capacitors or the requirement for a buffer to precede the filter. Its response is shown in Fig. 6.8 under 'A = 0'.

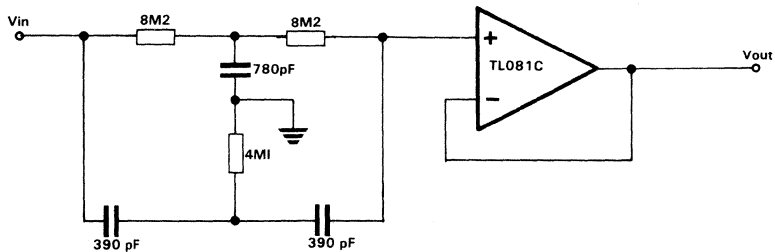
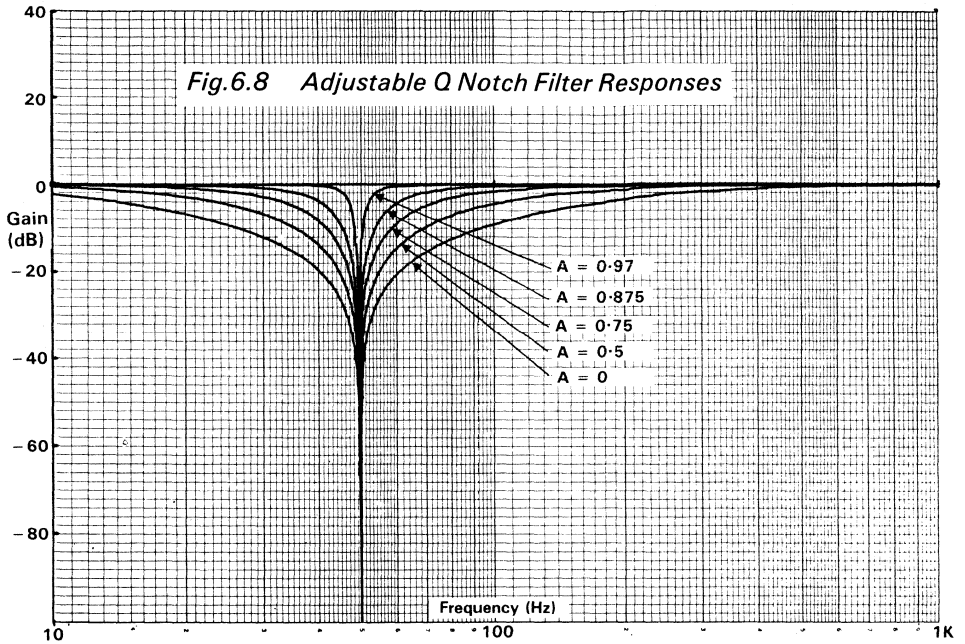
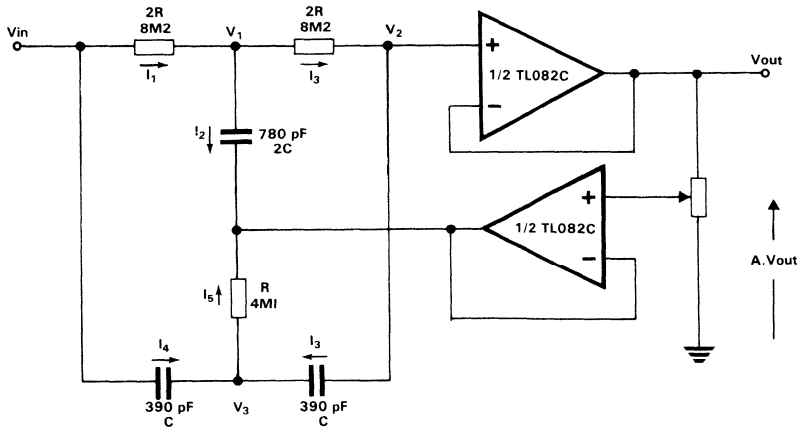


Fig. 6.7 'Twin T' 50Hz Notch Filter



Consider the variation shown in Fig. 6.9 where a second op amp has been added to feed a proportion,  $A$  ( $0 \leq A < 1$ ), of the output back to a node that was normally grounded.



**Fig. 6.9 Adjustable Q Notch Filter**

$$\text{From Fig. 6.9 } I_1 = \frac{V_{in} - V_1}{2R} \quad 1.$$

$$I_2 = (V_1 - AV_2) s \times 2C \quad 2.$$

$$I_3 = \frac{V_1 - V_2}{2R} = (V_2 - V_3) sC \quad 3.$$

$$I_4 = (V_{in} - V_3) sC \quad 4.$$

$$I_5 = \frac{V_3 - AV_2}{R} \quad 5.$$

$$\text{Also } I_2 + I_3 = I_1 \quad 6.$$

$$\text{and } I_3 + I_4 = I_5 \quad 7.$$

From 6, 1, 2 and 3

$$(V_1 - AV_2) 4sRC = V_{in} + V_2 - 2V_1 \quad 8.$$

From 3

$$V_1 = (V_2 - V_3) 2sRC + V_2 \quad 9.$$

Substituting 9 in 8

$$[(V_2 - V_3) 2sRC - (A - 1)V_2] 4sRC = V_{in} - V_2 - (V_2 - V_3) 4sRC \quad 10.$$

$(V_2 - V_3)$  must be eliminated from 10

∴ From 7, 3, 4 and 5

$$\frac{V_3 - AV_2}{sRC} = V_2 + V_{in} - 2V_3 \quad 11.$$

$$\therefore V_3 = \frac{V_{in} \times s \times RC + V_2 (sRC + A)}{1 + 2sRC} \quad 12.$$

$$(V_2 - V_3) = -(V_3 - V_2) \quad 13.$$

$$\therefore (V_2 - V_3) = - \left[ \frac{V_{in} \times s \times RC + V_2 (A - 1 - sRC)}{1 + 2sRC} \right] \quad 14.$$



Substituting 14 in 10 gives

$$V_{in} \times s \times RC + V_2 (A - 1 - sRC) = - (A - 1) V_2 + \frac{(V_2 - V_{in})}{4sRC} \quad 15.$$

which when re-arranged gives

$$\frac{V_2}{V_{in}} = \frac{V_{out}}{V_{in}} = \frac{4s^2R^2C^2 + 1}{4s^2R^2C^2 + (1 - A) 8sRC + 1} \quad 16.$$

This response is plotted in Fig. 6.8 for  $R = 4M\Omega$  and  $C = 390\text{pf}$  for various values of  $A$ . As can be predicted from equation 16 the transfer function goes to zero at a frequency of

$$\omega = \frac{1}{2RC} \quad \text{or} \quad F = \frac{1}{4\pi RC}$$

However it can also be seen that the  $Q$  of the notch is dependent upon the value of  $A$ .

It is interesting to see what happens when  $A = 1$ . Substituting this in equation 16 reveals that pole-zero cancellation occurs and the notch should become vanishingly small. In practice however this does not occur due to component mismatch and the fact that  $A$  never quite equals 1. The result is a notch with a high, but indeterminate,  $Q$  with possibly some peaking of the response close to the notch frequency. A still greater mismatch usually results in the circuit bursting into oscillation.

Consequently the circuit shown in Fig. 6.9 can be used to provide an adjustable  $Q$  notch but it is not good design practice to attempt to use the circuit with  $A = 1$ .

## 7. MISCELLANEOUS CIRCUITS

This section contains a number of circuits which have applications in general analogue systems. It also contains a short note on 'guard rings' as an aid for minimizing the errors due to circuit board leakage currents, in applications where the high impedance levels achievable using BIFET op amps may make these significant.

### 7.1 Capacitance Multiplier

In some circuits the need for large capacitor values can be eliminated by simply raising the general impedance level. However in some cases the impedance level is fixed by other considerations and hence it may be necessary to simulate a high capacitor value using a smaller value in conjunction with a capacitance multiplier.

In order to satisfactorily realise a very large capacitance value it must be ensured that the effective leakage current is less than that which would be obtained using, say, an extremely large tantalum capacitor.

A suitable circuit for a capacitance multiplier is given in Fig. 7.1.

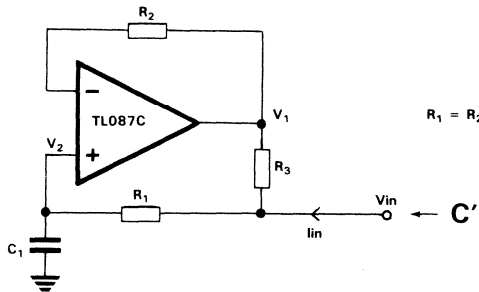


Fig. 7.1 Capacitance Multiplier

Assuming  $V_1 = V_2$  (unity gain buffer).

1.

$$I_{in} = \frac{V_{in} - V_1}{R_3} + \frac{V_{in} - V_2}{R_1}$$

2.

$$= (V_{in} - V_1) \left( \frac{1}{R_3} + \frac{1}{R_1} \right)$$

3.

But  $V_2 = V_1 = \frac{V_{in}}{1 + sR_1 \times C_1}$  if input impedance of + ve input can be neglected. (true for BIFET op amp).

4.

$$\therefore I_{in} = V_{in} \left( 1 - \frac{1}{1 + sR_1 \times C_1} \right) \left( \frac{1}{R_3} + \frac{1}{R_1} \right) \quad 5.$$

$$\therefore I_{in} = V_{in} \left( \frac{sR_1 \times C_1}{1 + sR_1 \times C_1} \right) \left( \frac{R_1 + R_3}{R_1 \times R_3} \right) \quad 6.$$

$$\therefore Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1 + sR_1 \times C_1}{sR_1 \times C_1} \left( \frac{R_1 \times R_3}{R_1 + R_3} \right) \quad 7.$$

$$Z_{in} = \frac{1}{s \times C_1} \left( \frac{R_1 + R_3}{R_3} \right) + \frac{R_1 \times R_3}{R_1 + R_3} \quad 8.$$

Hence  $C'$  is equivalent to a capacitance of  $C_1$  multiplied by a factor of  $\frac{R_1 + R_3}{R_3}$  in series with a resistance equal to  $R_1$  and  $R_3$  in parallel.

Unfortunately 1 is only approximately correct. The gain of the amplifier rolls off with frequency and hence the multiplication factor decreases and also becomes complex once the high frequency break point is approached. Fortunately this is not normally significant as frequencies of this order are seldom encountered in conjunction with circuits which require capacitor values in the 1mF region.

More importantly however is the d.c. offset between  $V_1$  and  $V_2$  which has a worst case value of  $V_{i0} + I_{i0} \times R_1$ . This gives rise to a current generator in parallel with  $C'$  having the value:

$$\frac{V_{i0} + I_{i0} \times R_1}{R_3} \quad \text{Amps}$$

Taking values from the data sheet for the TL087C and for  $R_1 = R_2 = 10M\Omega$  and  $R_3 = 1k\Omega$ ,  $C'$  takes the form shown in Fig. 7.2 since at  $25^\circ C$ ,  $V_{i0} < 0.5mV$ ,  $I_{i0} < 100pA$ .

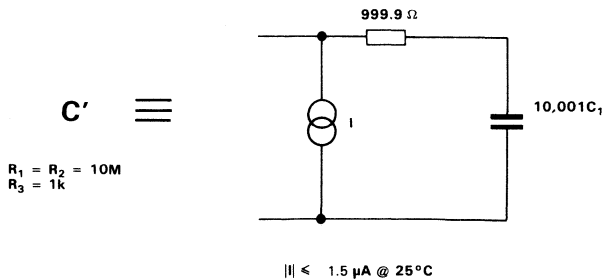


Fig. 7.2 Equivalent Circuit For  $C'$

The high effective series resistance precludes its use in high Q applications but the capacitance multiplier is extremely useful in timing circuits and such like.

## 7.2 Variable Capacitance Multiplier

Fig. 7.3 shows a circuit for a variable capacitance multiplier. The circuit operation is extremely simple and is very similar to the 'Miller' effect found in most active devices.

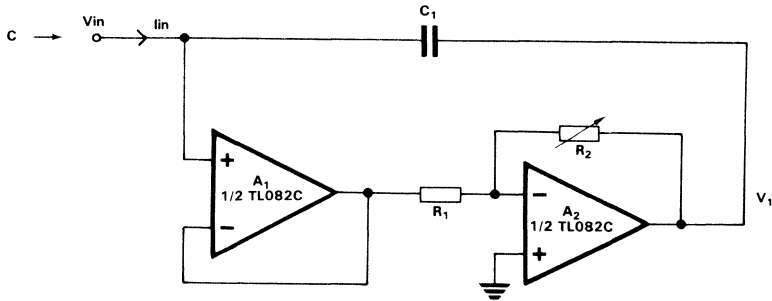


Fig. 7.3 Variable Capacitance Multiplier

A1 is used as a unity gain buffer and presents negligible loading on the input terminal. A2 is an inverting amplifier with a gain of  $-R_2/R_1$ .

$$\text{Thus } V_1 = -V_{in} \times \frac{R_2}{R_1}$$

$$I_{in} = (V_{in} - V_1) sC_1$$

$$\therefore Z_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{V_{in} \left(1 + \frac{R_2}{R_1}\right) sC_1}$$

$$Z_{in} = \frac{1}{sC_1 \times \left(\frac{R_2}{R_1} + 1\right)}$$

Thus the input terminal 'looks like' a capacitance of  $C_1 \times \left(\frac{R_2}{R_1} + 1\right)$ .

The effective series resistance of this multiplied value is purely the very small output resistance of A2 hence this circuit may be used in moderately high Q applications.

A practical point to be considered is that in many cases the maximum capacitance multiplication available is limited by the possibility of A2 output going into saturation.

### 7.3 Precision Current Sink

Fig. 7.4 shows one of the most common methods of producing a precision current sink.

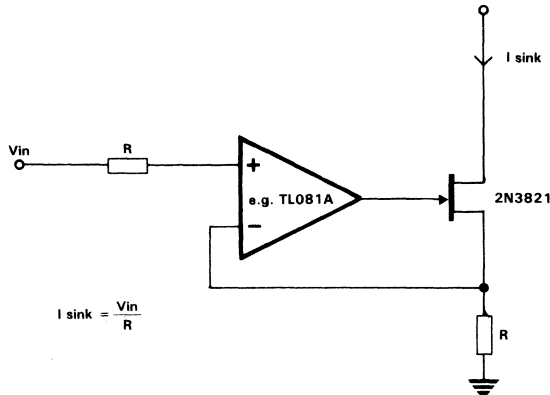


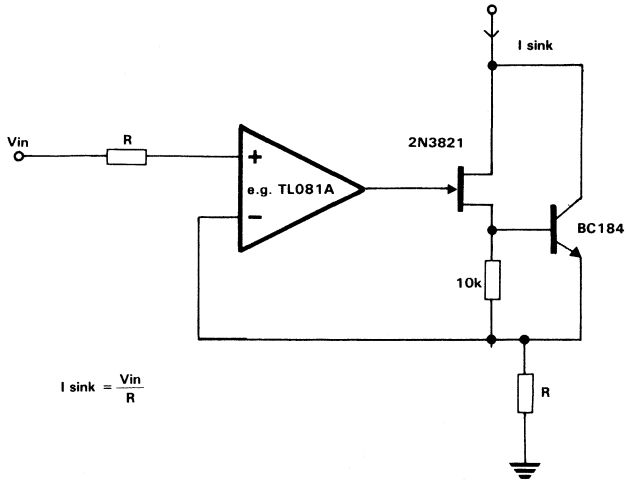
Fig. 7.4 Precision Current Sink

Difficulty is usually experienced when attempting to sink exceedingly small currents as the op amp bias currents often become significant (and sometimes the input offset voltage).

However using, for example, a TL081A the input offset current is typically 5 pA which is in the same order as the FET gate current. The input offset voltage is typically 3mV which may be externally nulled to zero if required. Thus currents in the order of nA may be generated with less than 1% error for input voltage in the order of 1V.

Fig. 7.5 shows a development of the circuit capable of handling currents up to 200mA. As in the previous circuit the order of magnitude of the sink current is set by the value of R whilst small variations can be made by changing Vin.

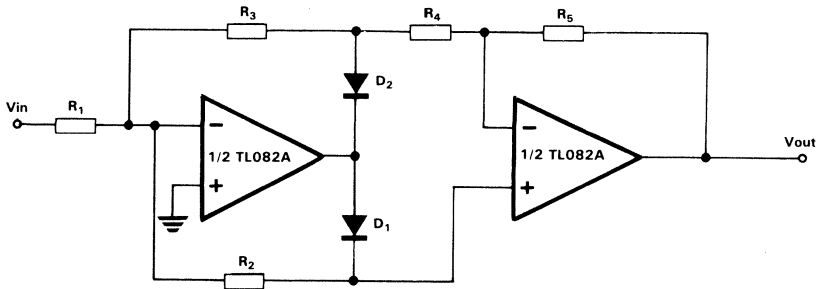
It should be noted that the maximum available power dissipation of the BC184 may limit the maximum sink current. If the 300mW limit (at 25°C) of the BC184 is insufficient then it may be replaced with a higher power transistor (preferably a darlington e.g. TIP120).



*Fig. 7.5 Precision Current Sink  
for  $I_{\text{sink}} \leq 200\text{mA}$*

### 7.4 Precision Full Wave Rectifier

Fig. 7.6 shows a precision full wave rectifier constructed from a TL082A dual BIFET operational amplifier.



*Fig. 7.6 Precision Full Wave Rectifier*

To understand the operation of the circuit consider the equivalent circuit under given polarity inputs.

1) +ve input

$D_1$  off and  $D_2$  on – see equivalent circuit in Fig. 7.7

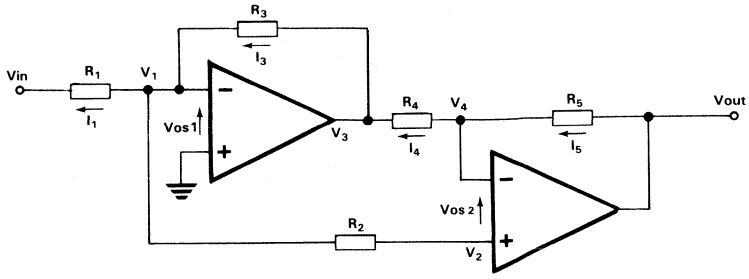


Fig. 7.7 Equivalent Circuit for +ve Inputs

$$I_1 = \frac{V_1 - V_{in}}{R_1} = I_3 = \frac{V_3 - V_1}{R_3} \quad 1.$$

$$I_4 = \frac{V_4 - V_3}{R_4} = I_5 = \frac{V_{out} - V_4}{R_5} \quad 2.$$

$$V_1 = V_2 \quad 3.$$

[1, 2 and 3 make usual assumptions about gain and bias currents etc.]

If all R's equal then

$$V_1 - V_{in} = V_3 - V_1 \quad 4.$$

and

$$V_4 - V_3 = V_{out} - V_4 \quad 5.$$

$$V_1 = V_{os1} \text{ and } V_4 = V_2 + V_{os2} = V_1 + V_{os2} = V_{os1} + V_{os2}$$

$$\text{From 4 } V_3 = -V_{in} + 2V_1 = -V_{in} + 2V_{os1} \quad 6.$$

$$\text{From 5 } V_{out} = -V_3 + 2V_4 = V_{in} - 2V_{os1} + 2V_{os2} + 2V_{os1}$$

$$\therefore \underline{V_{out} = V_{in} + 2V_{os2}}$$

2) -ve input

D<sub>1</sub> on and D<sub>2</sub> off – see equivalent circuit in Fig. 7.8

$$I_1 = \frac{V_1 - V_{in}}{R_1} = I_2 + I_3 = \frac{V_2 - V_1}{R_2} + \frac{V_4 - V_1}{R_3 + R_4} \quad 1.$$

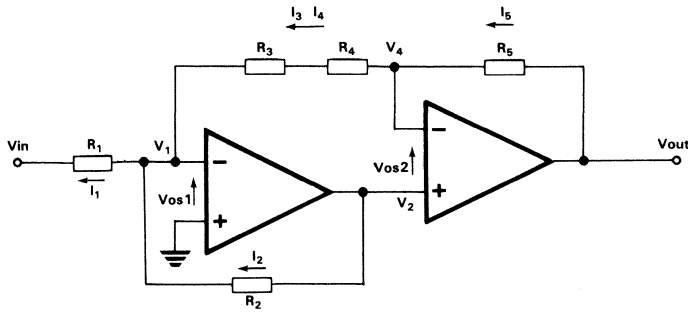


Fig. 7.8 Equivalent Circuit for  $-ve$  Inputs

But  $I_5 = I_{3,4}$  2.

$$\therefore \frac{V_{out} - V_4}{R_5} = \frac{V_4 - V_1}{R_3 + R_4}$$
 3.

[1, 2 and 3 make usual assumptions as for + ve inputs]

$$\therefore \frac{V_1 - V_{in}}{R_1} = \frac{V_2 - V_1}{R_2} + \frac{V_{out} - V_4}{R_5}$$
 4.

If all R's equal.

$$V_1 - V_{in} = V_2 - V_1 + V_{out} - V_4$$
 5.

Since  $V_1 = V_{os1}$  and  $V_4 = V_2 + V_{os2}$

$$V_{os1} - V_{in} = V_2 - V_{os1} + V_{out} - V_2 - V_{os2}$$
 6.

Hence  $V_{out} = -V_{in} + 2V_{os1} + V_{os2}$  7.

In both cases, ignoring offsets,

$$V_{out} = |V_{in}|$$

If the offsets as calculated above present too high a percentage error then either two single BIFET packages may be used, each with an external offset zero, or a type with a lower guaranteed offset should be used such as the TL287C.

When this circuit is used to rectify an a.c. waveform then it will be found that the high frequency performance is limited mainly by the slew rate of the first operational amplifier in Fig. 7.6. When the input is virtually zero (equal to the input offset voltage) the output of the op amp passes through zero and neither



$D_1$  nor  $D_2$  conducts. The op amp is then in an open loop state and this lasts until the output has 'slewed' across  $2V_{be}$ . This is illustrated in Fig. 7.9 and 7.10 which show output waveforms for input frequencies of 5kHz and 15kHz respectively.

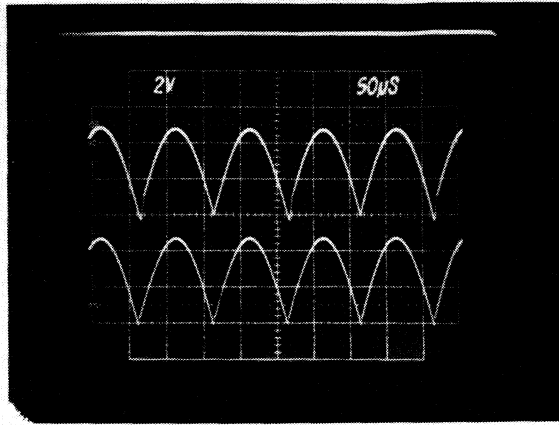


Fig. 7.9 Output Waveforms for  $f_{in} = 5\text{kHz}$

In each case the upper waveform was produced by replacing the TL082A with a standard bipolar op amp type LM2904P. This clearly shows the effect of slew rate limiting by the LM2904P and during testing it was found that using the TL082A, distortion of the form shown in Fig. 7.10 did not occur until frequencies in excess of 100kHz were applied.

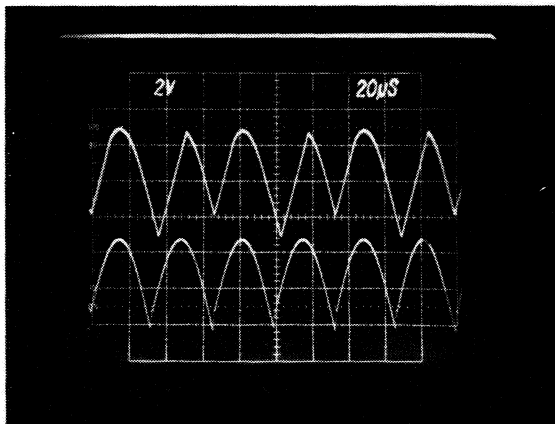


Fig. 7.10 Output Waveforms for  $f_{in} = 15\text{kHz}$

## 7.5 Simple Multimeter

The circuit shown in Fig. 7.11 was developed as a result of a requirement to monitor voltages between  $\pm 0.6V$  and  $\pm 600V$  from a high impedance source and also to measure currents from  $6nA$  to  $6\mu A$ . The resulting instrument was required to accept inputs of either polarity, have a long battery life, be inexpensive and above all be robust and reliable.

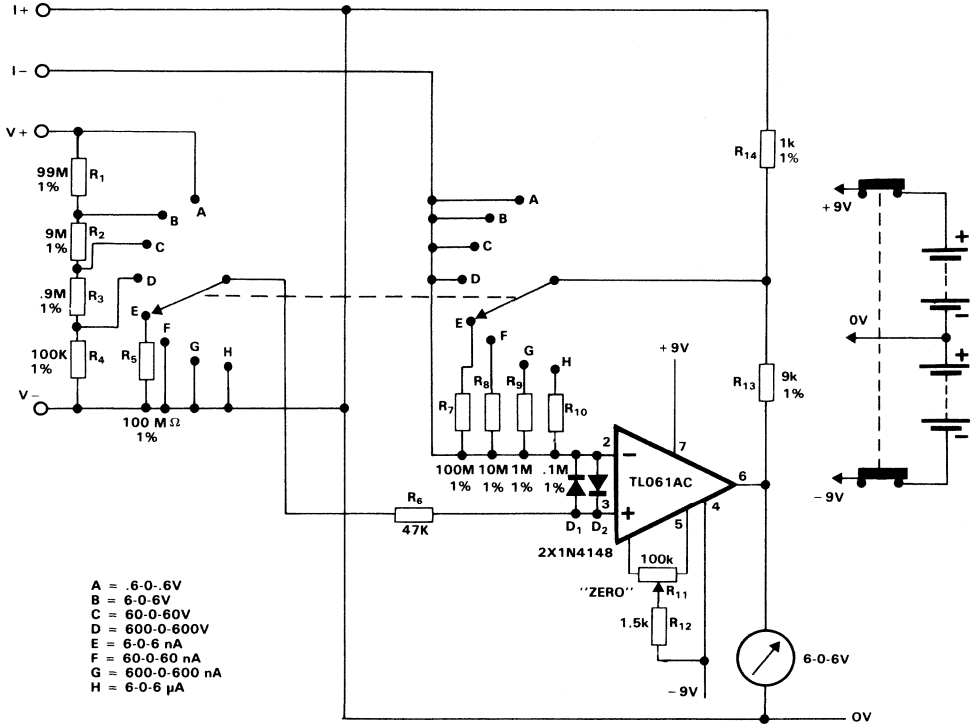


Fig. 7.11 Simple Multimeter

The lower power dissipation requirement dictated the use of either an LCD display or a simple analogue meter. Since absolute accuracy was not of prime importance, but cost effectiveness was, an inexpensive, centre zero meter was used.

The operational amplifier in Fig. 7.11 is one of the low power series which, with a no signal power requirement of  $7.5mW$  max, maximises the battery life.

For voltage measurements (switch positions A to D) the op amp is configured to have a non-inverting gain of 10 whilst range selection is achieved using a simple divider network, giving a fixed input impedance of  $100M\Omega$ . A panel mounted 'zero' control is included to facilitate corrections for the mechanical meter movement zero error and the op amp input offset voltage.

In the current measuring mode (switch positions E to H) the op amp operates as a current to voltage converter. For the most sensitive range of  $\pm 6\text{nA}$  a transimpedance of  $1\text{G}\Omega$  is required to produce full scale deflection of the meter. Accurate  $1\text{G}\Omega$  resistors are available, in glass packages, although they are notoriously difficult to apply. The effective resistance is often more dependent on the board layout and the moisture content of the surrounding air than on the resistor itself! Consequently a resistance multiplier arrangement was used in conjunction with a  $100\text{M}\Omega$  feedback resistor for the most sensitive range. The input offset current of the BIFET op amp ( $100\text{pA}$  max,  $5\text{pA}$  typ) is not significant and the effective output offset caused by this current, given by

$$\begin{aligned} & 100\text{pA} \times 100\text{M}\Omega \times 10 \\ & = 0.1\text{V max (0.005V typ)} \end{aligned}$$

is easily compensated for by the zero control. On less sensitive ranges the effect of the bias currents is totally negligible and hence no bias current compensation resistors, other than  $R_5$ , were included.

Protection against gross overloads on both voltage and current measuring ranges is provided by  $R_6$  in conjunction with the two diodes  $D_1$  and  $D_2$ .

Although not contained on the original design it is feasible to insert the precision full-wave rectifier described earlier at the output of the TL061AC and replace the centre zero meter with a single polarity type. Polarity indication could be generated by a simple comparator at the output of the TL061AC.

This arrangement would also allow measurement of a.c. signals, although the input divider network would require frequency compensation to allow for the roll-off produced by stray capacitances reacting with the very high impedances.

## 7.6 Guard Rings

BIFET operational amplifier applications are very often associated with high impedance circuits. The extremely small bias currents of these devices allow impedances in the order of  $10^9\Omega$  to be utilised without significant errors. However at this sort of level circuit board leakages can easily cause more errors than that due to the op amp itself. PCBs should be thoroughly cleaned in a suitable solvent to remove solder fluxes and carefully dried. They should then be coated with epoxy or silicon rubber. Silicon rubber is by far the easiest to use, but for better durability and resistance against contamination epoxy is to be preferred, provided that it is properly cured.

Even with properly cleaned and coated boards, for critical high impedance applications, it is wise to minimise the possibility of error by the suitable use of guard rings.

A guard ring takes the form of a piece of track on the PCB which totally encloses the sensitive input. If this track can be driven by a low impedance source to the

same voltage as the input then obviously leakage currents are greatly diminished. Fig. 7.12 shows how this may be achieved for a simple voltage follower. A bias current compensation resistor has been included and the voltage between the guard ring and the inputs can be made of the same order as the input offset voltage thus greatly reducing leakage currents. Fig. 7.13 and 7.14 show similar arrangements for an inverting and non-inverting amplifier. In each case the secret is to maintain the guard ring at the same potential as the inputs, whether it be at 0V in the case of an inverting amplifier or equal to the input voltage for a non inverting case.

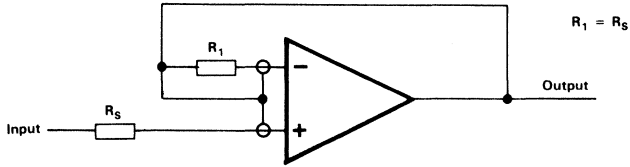


Fig. 7.12 Guarding Voltage Follower Inputs

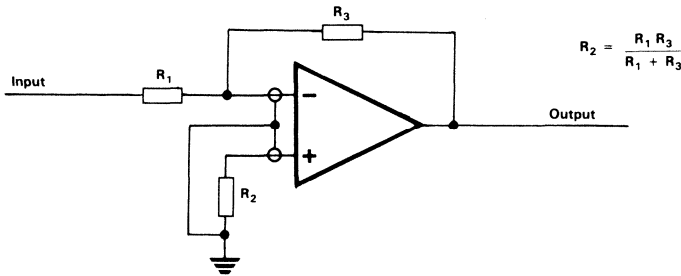


Fig. 7.13 Guarding Inverting Amplifier Inputs

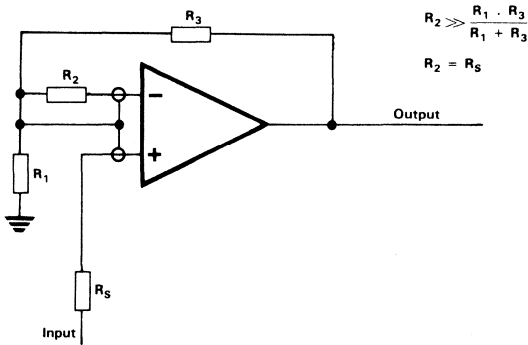


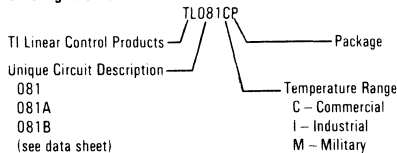
Fig. 7.14 Guarding Non-inverting Amplifier Inputs

# The BIFET families

		TLO61 SERIES	TLO71 SERIES	TLO81 SERIES	TLO87 SERIES
		LOW POWER	LOW NOISE	GENERAL PURPOSE	LOW OFFSET
<b>SINGLES</b>	<ul style="list-style-type: none"> <li>EXTERNAL FREQUENCY COMPENSATION</li> <li>OFFSET NULL CAPABILITIES</li> </ul> $\mu$ A748, TYPE PINOUT	TLO60CP* TLO600IP TLO60CJG* TLO600JG TLO60ACP TLO60MJG* TLO60AGJG	TLO70CP* TLO700IP TLO70CJG* TLO700JG TLO70ACP TLO70MJG* TLO70ACJG	TLO80CP* TLO800IP TLO80CJG* TLO800JG TLO80MJG*	
	<ul style="list-style-type: none"> <li>INTERNAL FREQUENCY COMPENSATION</li> <li>EXTERNAL OFFSET CONTROL</li> </ul> $\mu$ A741, TYPE PINOUT	TLO61CP* TLO610IP TLO61CJG* TLO610JG TLO61ACP* TLO61MJG* TLO61ACJG TLO61MJG* TLO61BCP* TLO610JG TLO61BCJG	TLO71CP* TLO710CJG TLO71CJG* TLO710IP TLO71ACP* TLO710JG TLO71ACJG TLO71MJG* TLO71BCP*	TLO81CP* TLO810CJG TLO81CJG* TLO810IP TLO811P TLO810JG TLO81MJG*	TLO87CP* TLO88MJG TLO88CP* TLO87CJG* TLO88CJG* TLO87IP TLO88IP TLO87JG TLO88JG
<b>DUALS</b>	<ul style="list-style-type: none"> <li>INTERNAL FREQUENCY COMPENSATION</li> </ul> MC1458, RC4558, TYPE PINOUT	TLO62CP* TLO620IP TLO62CJG* TLO620JG TLO62ACP* TLO62MJG* TLO62ACJG TLO62MJG* TLO62BCP* TLO620JG TLO62BCJG	TLO72CP* TLO720IP TLO72CJG* TLO720JG TLO72ACP* TLO72MJG* TLO72ACJG TLO72MJG* TLO72BCP* TLO720JG TLO72BCJG	TLO82CP* TLO820CJG TLO82CJG* TLO820IP TLO82IP TLO820JG TLO82MJG*	TL287CP* TL288MJG TL288CP* TL287CJG* TL288CJG* TL287IP TL288IP TL287JG TL288JG
	$\mu$ A747, TYPE PINOUT			TLO83CN* TLO830IN TLO83CJ TLO830J	
<b>QUADS</b>	LM324, TYPE PINOUT	TLO64CN* TLO648CN* TLO64CJ* TLO648CJ TLO64ACN* TLO640IN TLO64ACJ TLO640J TLO64MJ*	TLO74CN* TLO748CN* TLO74CJ* TLO748CJ TLO74ACN* TLO740IN TLO74ACJ TLO740J TLO74MJ	TLO84CN* TLO840IN TLO84CJ* TLO84MJ*	
	RC4136, TYPE PINOUT		TLO75CN	TLO85CN	
<b>MISCELLANEOUS BIFET PRODUCTS</b>		TLO66CP* TLO660IP TLO66 IS IDENTICAL TO THE TLO61 TLO66CJG* TLO660JG EXCEPT A POWER CONTROL FUNCTION TLO66ACP* ON PIN 8 IS AVAILABLE ON THE TLO66 TLO66BCP*  TLO68CLP* A 3 PIN VOLTAGE FOLLOWER SIMILAR TO UNITY GAIN TLO61			

\*Preferred Typ

## Ordering Information



# LINEAR INTEGRATED CIRCUITS

# TYPES TL060, TL060A, TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

BULLETIN NO. DLS 12647, NOVEMBER 1978

19 DEVICES COVER COMMERCIAL,  
INDUSTRIAL, AND MILITARY  
TEMPERATURE RANGES

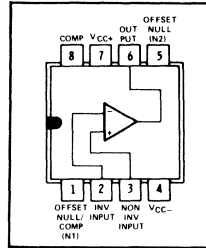
- Very Low Power Consumption
- Typical Supply Current . . . 200  $\mu$ A
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 3.5 V/ $\mu$ s Typ

## description

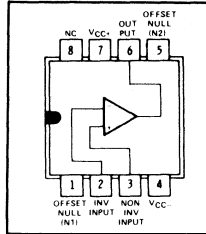
The JFET-input operational amplifiers of the TL061 series are designed as low-power versions of the TL081 series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The TL061 series features the same terminal assignments as the TL071 and TL081 series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Device types with an "M" suffix are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , those with an "I" suffix are characterized for operation from  $-25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , and those with a "C" suffix are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

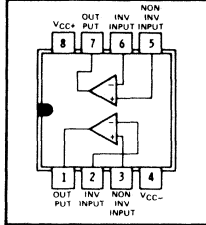
TL060, TL060A  
JG OR P DUAL-IN-LINE  
PACKAGE (TOP VIEW)



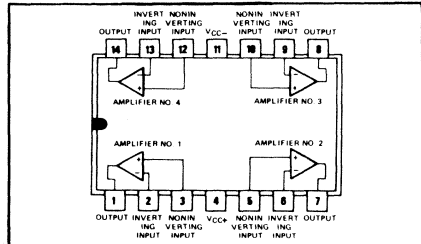
TL061, TL061A, TL061B  
JG OR P DUAL-IN-LINE  
PACKAGE (TOP VIEW)



TL062, TL062A, TL062B  
JG OR P DUAL-IN-LINE  
PACKAGE (TOP VIEW)



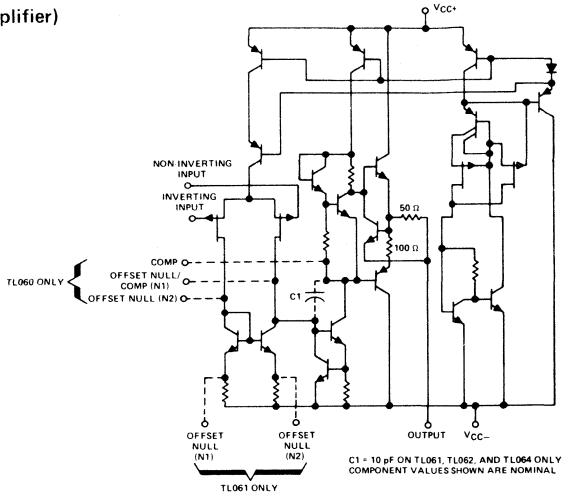
TL064, TL064A, TL064B  
J OR N DUAL-IN-LINE  
PACKAGE (TOP VIEW)



NC: No internal connection

# TYPES TL060, TL060A, TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL06_M	TL06_I	TL06_C TL06_AC TL06_BC	UNIT
Supply voltage, $V_{CC+}$ (see Note 1)	18	18	18	V
Supply voltage, $V_{CC-}$ (see Note 1)	-18	-18	-18	V
Differential input voltage (see Note 2)	$\pm 30$	$\pm 30$	$\pm 30$	V
Input voltage (see Notes 1 and 3)	$\pm 15$	$\pm 15$	$\pm 15$	V
Duration of output short circuit (see Note 4)	Unlimited	Unlimited	Unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	680	680	680	mW
Operating free-air temperature range	-55 to 125	-25 to 85	0 to 70	°C
Storage temperature range	-65 to 150	-65 to 150	-65 to 150	°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds	J or JG Package	300	300	°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	N or P Package	260	260	°C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C, free air temperature, refer to Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE $T_A$
J	680 mW	8.2 mW/°C	67°C
JG	680 mW	6.6 mW/°C	47°C
N	680 mW	9.2 mW/°C	76°C
P	680 mW	8.0 mW/°C	65°C

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TL060	TL061	TL062	TL064
TL06_M	JG	JG	JG	J
TL06_I	JG, P	JG, P	JG, P	J, N
TL06_C	JG, P	JG, P	JG, P	J, N
TL06_AC	JG, P	JG, P	JG, P	J, N
TL06_BC	JG, P	JG, P	JG, P	J, N

# TYPES TL060, TL060A, TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

electrical characteristics,  $V_{CC\pm} = \pm 15$  V

PARAMETER	TEST CONDITIONS†		TL06_M		TL06_I		TL06_C TL06_AC TL06_BC		UNIT	
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX		
$V_{IO}$ Input offset voltage	$R_S = 50 \Omega$ , $T_A = 25^\circ\text{C}$	'60, '61, '62	3	6	3	6	3	15	mV	
		'64	3	9	3	6	3	15		
		'60A, '61A, '62A, '64A						3		6
	'61B, '62B, '64B							2		3
	$R_S = 50 \Omega$ , $T_A = \text{full range}$	'60, '61, '62		9		9		20		
		'64		15		9		20		
'60A, '61A, '62A, '64A							7.5			
'61B, '62B, '64B							5			
$\alpha V_{IO}$ Temperature coefficient of input offset voltage	$R_S = 50 \Omega$ , $T_A = \text{full range}$		10		10		10	$\mu\text{V}/^\circ\text{C}$		
$I_{IO}$ Input offset current‡	$T_A = 25^\circ\text{C}$	'60, '61, '62, '64	5	100	5	100	5	200	pA	
		'60A, '61A, '62A, '64A					5	100		
		'61B, '62B, '64B					5	100		
	$T_A = \text{full range}$	'60, '61, '62, '64		20		10		5	nA	
'60A, '61A, '62A, '64A							3			
'61B, '62B, '64B							3			
$I_{IB}$ Input bias current‡	$T_A = 25^\circ\text{C}$	'60, '61, '62, '64	30	200	30	200	30	400	pA	
		'60A, '61A, '62A, '64A					30	200		
		'61B, '62B, '64B					30	200		
	$T_A = \text{full range}$	'60, '61, '62, '64		50		20		10	nA	
'60A, '61A, '62A, '64A							7			
'61B, '62B, '64B							7			
$V_{ICR}$ Common-mode input voltage range*	$T_A = 25^\circ\text{C}$	'60, '61, '62, '64	$\pm 11$	$\pm 12$	$\pm 11.5$	$\pm 12$	$\pm 10$	$\pm 11$	V	
		'60A, '61A, '62A, '64A					$\pm 11.5$	$\pm 12$		
		'61B, '62B, '64B					$\pm 11.5$	$\pm 12$		
$V_{OPP}$ Maximum peak-to-peak output voltage swing	$T_A = 25^\circ\text{C}$ , $R_L = 10 \text{ k}\Omega$		20	27	20	27	20	27	V	
	$T_A = \text{full range}$ , $R_L \geq 10 \text{ k}\Omega$		20		20		20			
$A_{VD}$ Large-signal differential voltage amplification	$R_L \geq 10 \text{ k}\Omega$ , $V_O = \pm 10 \text{ V}$ , $T_A = 25^\circ\text{C}$	'60, '61, '62, '64	4	6	4	6	3	6	V/mV	
		'60A, '61A, '62A, '64A					4	6		
		'61B, '62B, '64B					4	6		
		$R_L \geq 10 \text{ k}\Omega$ , $V_O = \pm 10 \text{ V}$ , $T_A = \text{full range}$	'60, '61, '62, '64	4		4		3		
		'60A, '61A, '62A, '64A					4			
'61B, '62B, '64B					4					
$B_1$ Unity-gain bandwidth	$T_A = 25^\circ\text{C}$ , $R_L = 10 \text{ k}\Omega$		1		1		1	MHz		
$r_i$ Input resistance	$T_A = 25^\circ\text{C}$		$10^{12}$		$10^{12}$		$10^{12}$	$\Omega$		
CMRR Common-mode rejection ratio	$R_S \leq 10 \text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	'60, '61, '62, '64	80	86	80	86	70	76	dB	
		'60A, '61A, '62A, '64A					80	86		
		'61B, '62B, '64B					80	86		
$k_{SVR}$ Supply voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$R_S \leq 10 \text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	'60, '61, '62, '64	80	95	80	95	70	95	dB	
		'60A, '61A, '62A, '64A					80	95		
		'61B, '62B, '64B					80	95		
$P_D$ Total power dissipation (each amplifier)	No load, $T_A = 25^\circ\text{C}$	No signal,	6	7.5	6	7.5	6	7.5	mW	
$I_{CC}$ Supply current (each amplifier)	No load,	No signal,	200	250	200	250	200	250	$\mu\text{A}$	
	$T_A = 25^\circ\text{C}$									
$V_{O1}/V_{O2}$ Channel separation	$A_{VD} = 100$ , $T_A = 25^\circ\text{C}$		120		120		120		dB	

† All characteristics are specified under open-loop conditions unless otherwise noted. Full range for  $T_A$  is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for TL06\_M;  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  for TL06\_I, and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for TL06\_C, TL06\_AC, and TL06\_BC.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

\* The  $V_{ICR}$  limits are directly linked volt-for-volt to supply voltage, viz the limit is 4 volts less than  $|V_{CC\pm}|$ .



# TYPES TL060, TL060A, TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$S_R$ Slew rate at unity gain	$V_I = 10\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , See Figure 1		3.5		$\text{V}/\mu\text{s}$
$t_r$ Rise time	$V_I = 20\text{ mV}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , See Figure 1		0.2		$\mu\text{s}$
Overshoot factor	$C_L = 100\text{ pF}$ , See Figure 1		10%		
$V_n$ Equivalent input noise voltage	$R_S = 100\ \Omega$ , $f = 1\text{ kHz}$		42		$\text{nV}/\sqrt{\text{Hz}}$

## PARAMETER MEASUREMENT INFORMATION

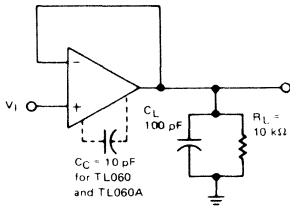


FIGURE 1—UNITY-GAIN AMPLIFIER

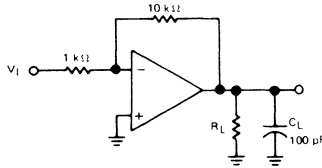


FIGURE 2—GAIN-OF-10  
INVERTING AMPLIFIER

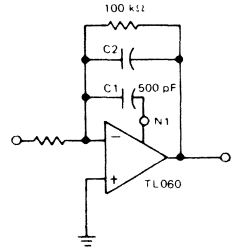
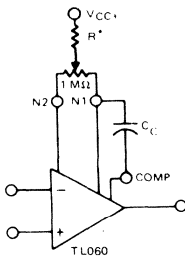


FIGURE 3—FEED-FORWARD  
COMPENSATION

## INPUT OFFSET VOLTAGE NULL CIRCUIT



\* For best results use  $R = 20\text{ M}\Omega$  for  $V_{CC\pm} = \pm 15\text{ V}$  to  $R = 5\text{ M}\Omega$  for  $V_{CC\pm} = \pm 3\text{ V}$ .

FIGURE 4

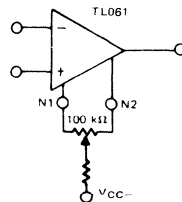


FIGURE 5

# TYPES TL060, TL060A, TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B

## LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

### TYPICAL CHARACTERISTICS†

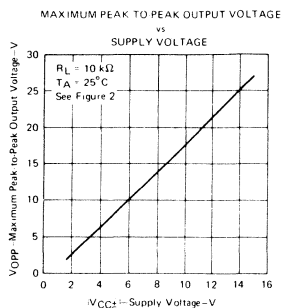


FIGURE 6

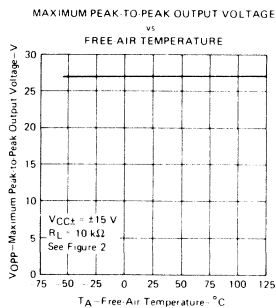


FIGURE 7

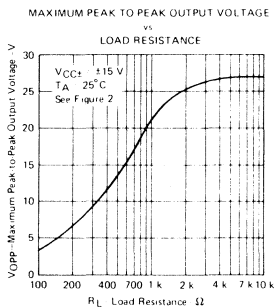


FIGURE 8

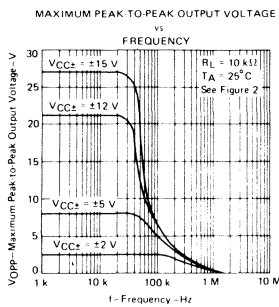


FIGURE 9

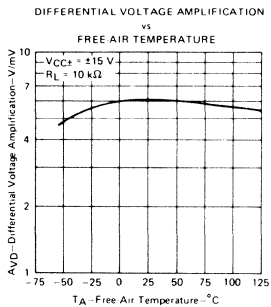


FIGURE 10

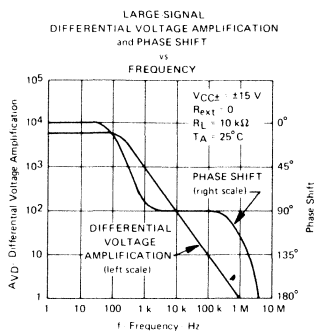


FIGURE 11

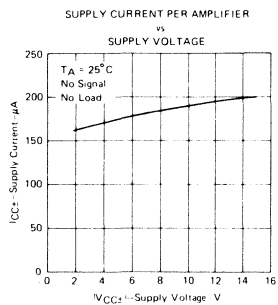


FIGURE 12

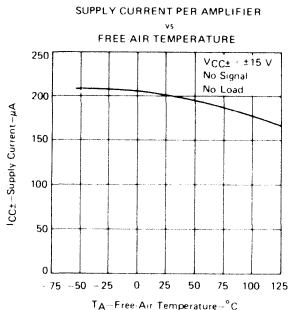


FIGURE 13

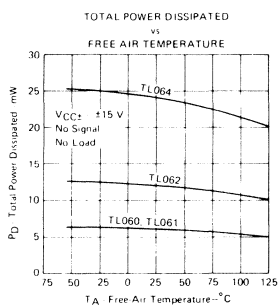


FIGURE 14

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 10-pF compensation capacitor is used with TL060 and TL060A.

# TYPES TL060, TL060A, TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

## TYPICAL CHARACTERISTICS†

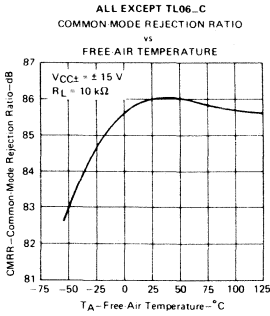


FIGURE 15

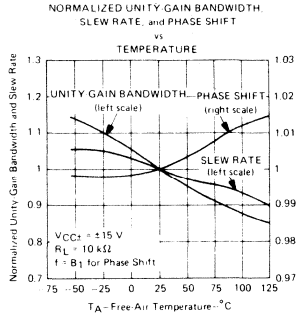


FIGURE 16

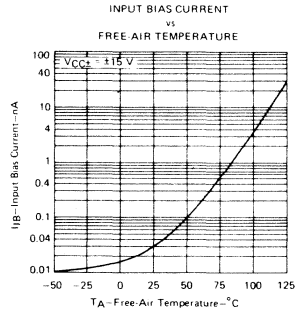


FIGURE 17

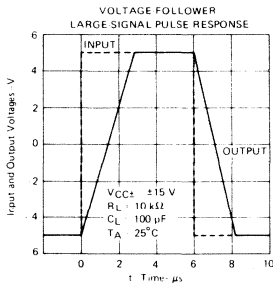


FIGURE 18

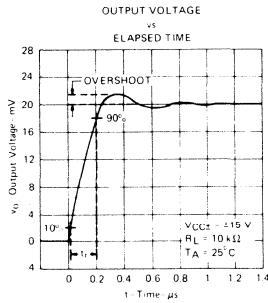


FIGURE 19

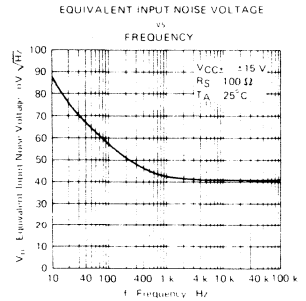


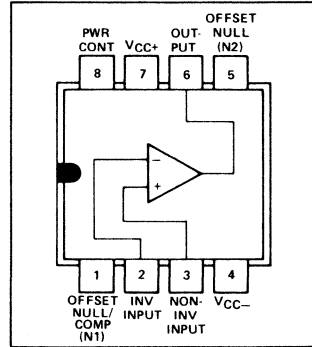
FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 10-pF compensation capacitor is used with TL060 and TL060A.

**5 DEVICES COVER COMMERCIAL,  
INDUSTRIAL, AND MILITARY  
TEMPERATURE RANGES**

- Very Low Adjustable ("Programmable") Power Consumption
- Adjustable Supply Current . . . 5 to 200  $\mu$ A
- Very Low Input Bias and Offset Currents
- Wide Supply Range . . .  $\pm 1.2$  V to  $\pm 18$  V
- Wide Common-Mode and Differential Voltage Ranges
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Typ Unity-Gain Bandwidth . . . 1 MHz (100 kHz at 25  $\mu$ W)
- High Slew Rate . . . 3.5 V/ $\mu$ s Typ
- Internal Frequency Compensation
- Latch-Up-Free Operation

TL066, TL066A, TL066B  
JG OR P DUAL-IN-LINE  
PACKAGE (TOP VIEW)



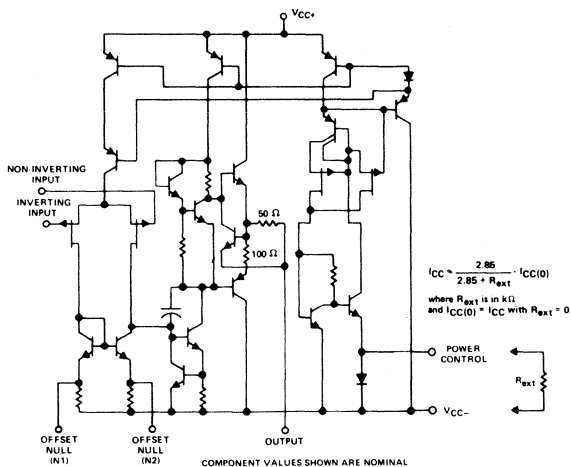
**description**

The TL066, TL066A, and TL066B are JFET-input operational amplifiers similar to the TL061 with the additional feature of being power-adjustable. They feature very low input offset and bias currents, high input impedance, wide bandwidth, and high slew rate. The power-control feature permits the amplifiers to be adjusted to require as little as 25 microwatts of power. This type of amplifier, which provides for changing several characteristics by varying one external element, is sometimes referred to as being "programmable". The JFET input stage combined with the adjustable-low-power feature results in superior bandwidth and slew rate performance compared to low-power bipolar-input devices.

The TL066M is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , the TL066I is characterized for operation from  $-25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , and the TL066C, TL066AC, and TL066BC are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

# TYPES TLO66M, TLO66I, TLO66C, TLO66AC, TLO66BC ADJUSTABLE LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TLO66M	TLO66I	TLO66C TLO66AC TLO66BC	UNIT
Supply voltage, $V_{CC+}$ (see Note 1)	18	18	18	V
Supply voltage, $V_{CC-}$ (see Note 1)	-18	-18	-18	V
Differential input voltage (see Note 2)	$\pm 30$	$\pm 30$	$\pm 30$	V
Input voltage (see Notes 1 and 3)	$\pm 15$	$\pm 15$	$\pm 15$	V
Voltage between power-control terminal and $V_{CC-}$	$\pm 0.5$	$\pm 0.5$	$\pm 0.5$	V
Duration of output short circuit (see Note 4)	Unlimited	Unlimited	Unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	680	680	680	mW
Operating free-air temperature range	-55 to 125	-25 to 85	0 to 70	°C
Storage temperature range	-65 to 150			°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds	JG Package	300	300	°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	P Package		260	°C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C, free air temperature, refer to Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE $T_A$
JG	680 mW	6.6 mW/°C	47°C
P	680 mW	8.0 mW/°C	65°C

# TYPES TL066M, TL066I, TL066C, TL066AC, TL066BC

## ADJUSTABLE LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

electrical characteristics,  $V_{CC\pm} = \pm 15 \text{ V}$

PARAMETER	TEST CONDITIONS†		TL066M			TL066I			TL066C TL066AC TL066BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$R_S = 50 \Omega$ , $T_A = 25^\circ\text{C}$	TL066	3	6		3	6		3	15	mV	
		TL066A							3	6		
		TL066B							2	3		
	$R_S = 50 \Omega$ , $T_A = \text{full range}$	TL066		9			9			20		
		TL066A								7.5		
		TL066B								5		
$\alpha V_{IO}$ Temperature coefficient of input offset voltage	$R_S = 50 \Omega$ , $T_A = \text{full range}$		20			20			20	$\mu\text{V}/^\circ\text{C}$		
$I_{IO}$ Input offset current‡	$T_A = 25^\circ\text{C}$	TL066	5	100		5	100		5	200	pA	
		TL066A							5	100		
		TL066B							5	100		
	$T_A = \text{full range}$	TL066		20			10			5	nA	
		TL066A								3		
		TL066B								3		
$I_{IB}$ Input bias current‡	$T_A = 25^\circ\text{C}$	TL066	30	200		30	200		30	400	pA	
		TL066A							30	200		
		TL066B							30	200		
	$T_A = \text{full range}$	TL066		50			20			10	nA	
		TL066A								7		
		TL066B								7		
$V_{ICR}$ Common-mode input voltage range*	$T_A = 25^\circ\text{C}$	TL066	$\pm 11$	$\pm 12$		$\pm 12$	$\pm 12$		$+10$	$\pm 11$	V	
		TL066A								$\pm 12$		$\pm 12$
		TL066B								$\pm 12$		$\pm 12$
$V_{OPP}$ Maximum peak-to-peak output voltage swing	$T_A = 25^\circ\text{C}$	$R_L = 10 \text{ k}\Omega$	20	27		20	27		20	27	V	
	$T_A = \text{full range}$ , $R_L \geq 10 \text{ k}\Omega$		20			20			20			
$A_{VD}$ Large-signal differential voltage amplification	$R_L \geq 10 \text{ k}\Omega$ , $V_O = +10 \text{ V}$ , $T_A = 25^\circ\text{C}$	TL066	4	6		4	6		3	6	V/mV	
		TL066A							4	6		
		TL066B							4	6		
		$R_L \geq 10 \text{ k}\Omega$ , $V_O = +10 \text{ V}$ , $T_A = \text{full range}$	TL066	4			4			3		
			TL066A							4		
			TL066B							4		
$B_1$ Unity-gain bandwidth	$T_A = 25^\circ\text{C}$ , $R_L = 10 \text{ k}\Omega$		1			1			1	MHz		
$r_i$ Input resistance	$T_A = 25^\circ\text{C}$		$10^{12}$			$10^{12}$			$10^{12}$	$\Omega$		
$r_o$ Output resistance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ kHz}$		220			220			220	$\Omega$		
CMRR Common-mode rejection ratio	$R_S \leq 10 \text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	TL066	80	86		80	86		70	76	dB	
		TL066A							80	86		
		TL066B							80	86		
$k_{SVR}$ Supply voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$R_S \leq 10 \text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	TL066	80	95		80	95		70	95	dB	
		TL066A							80	95		
		TL066B							80	95		
$P_D$ Total power dissipation	No load, $T_A = 25^\circ\text{C}$ ,	No signal,	6	7.5		6	7.5		6	7.5	mW	
$I_{CC}$ Supply current	No load, $T_A = 25^\circ\text{C}$ ,	No signal,	200	250		200	250		200	250	$\mu\text{A}$	

† All characteristics are specified under open-loop conditions unless otherwise noted. Full range for  $T_A$  is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for TL066M;  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  for TL066I; and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for TL066C, TL066AC, and TL066BC. The electrical parameters are measured with the power-control terminal (pin B) connected to  $V_{CC-}$ .

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

\* The  $V_{ICR}$  limits are directly linked volt to supply voltage, viz the limit is 4 volts less than  $|V_{CC\pm}|$ .

# TYPES TLO66M, TLO66I, TLO66C, TLO66AC, TLO66BC ADJUSTABLE LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_{\text{ext}} = 0$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , See Figure 1		3.5		$\text{V}/\mu\text{s}$
$t_r$	Rise time	$V_I = 20\text{ mV}$ , $R_L = 10\text{ k}\Omega$		0.2		$\mu\text{s}$
	Overshoot factor	$C_L = 100\text{ pF}$ , See Figure 1		10%		
$V_n$	Equivalent input noise voltage	$R_S = 100\ \Omega$ , $f = 1\text{ kHz}$		42		$\text{nV}/\sqrt{\text{Hz}}$

## PARAMETER MEASUREMENT INFORMATION

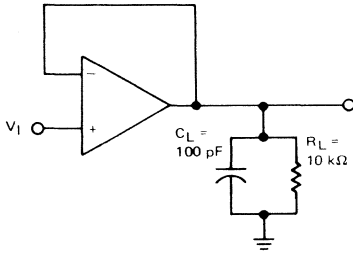


FIGURE 1—UNITY-GAIN AMPLIFIER

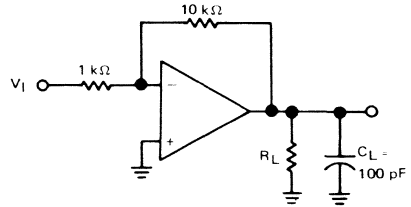


FIGURE 2—GAIN-OF-10 INVERTING AMPLIFIER

## INPUT OFFSET VOLTAGE NULL CIRCUIT

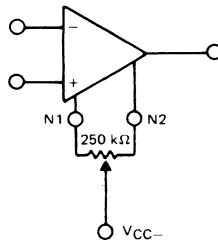


FIGURE 3

# TYPES TL066M, TL066I, TL066C, TL066AC, TL066BC ADJUSTABLE LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

## TYPICAL CHARACTERISTICS†

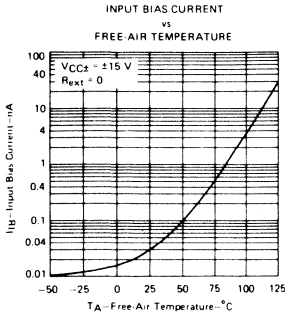


FIGURE 4

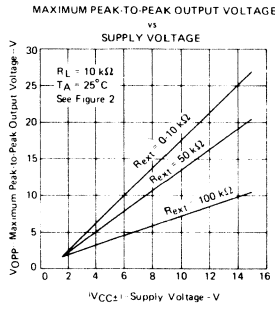


FIGURE 5

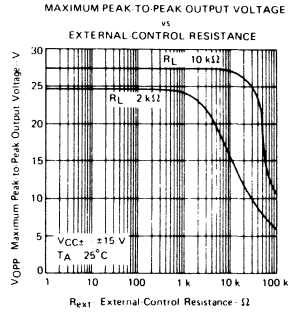


FIGURE 6

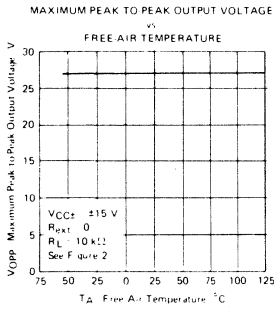


FIGURE 7

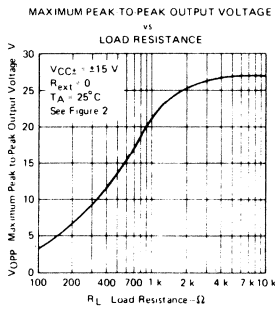


FIGURE 8

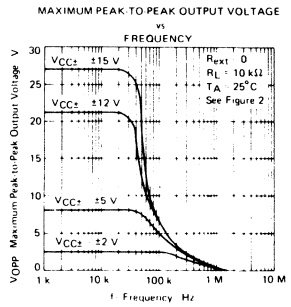


FIGURE 9

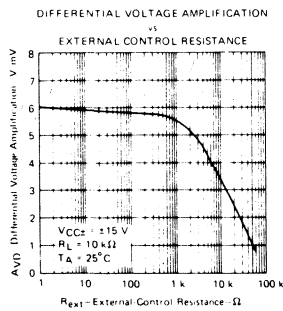


FIGURE 10

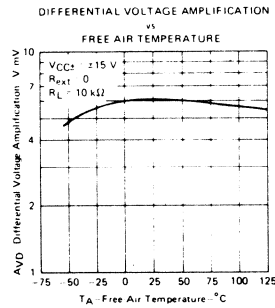


FIGURE 11

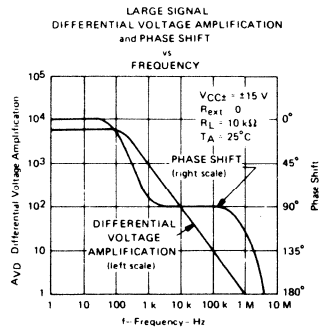


FIGURE 12

† Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.



# TYPES TLO66M, TLO66I, TLO66C, TLO66AC, TLO66BC

## ADJUSTABLE LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

### TYPICAL CHARACTERISTICS†

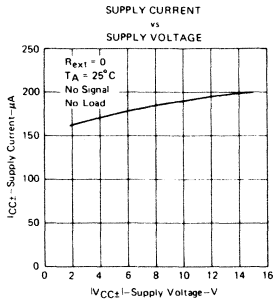


FIGURE 13

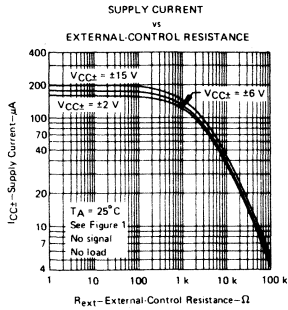


FIGURE 14

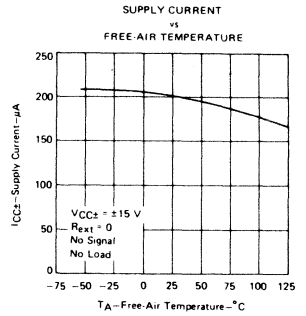


FIGURE 15

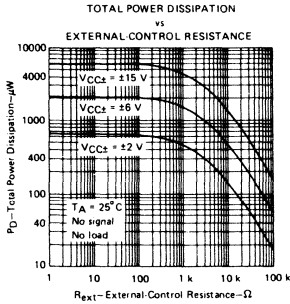


FIGURE 16

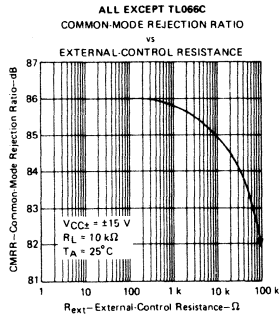


FIGURE 17

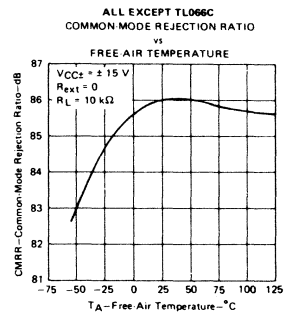


FIGURE 18

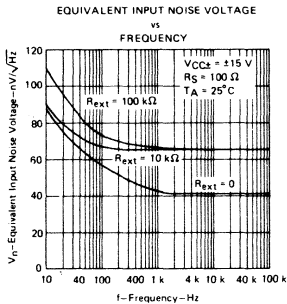


FIGURE 19

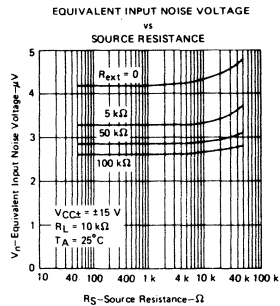


FIGURE 20

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

# TYPES TLO66M, TLO66I, TLO66C, TLO66AC, TLO66BC ADJUSTABLE LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

## TYPICAL CHARACTERISTICS†

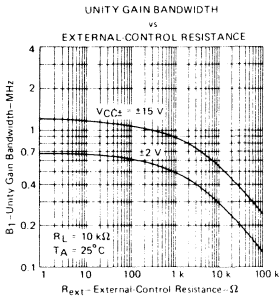


FIGURE 21

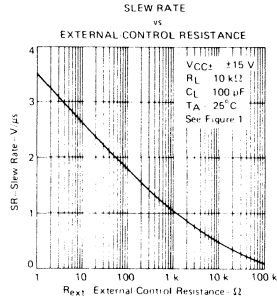


FIGURE 22

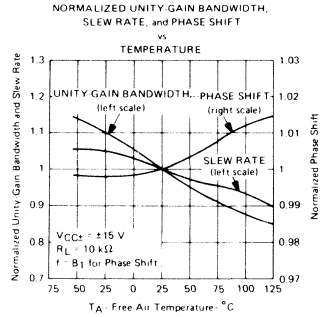


FIGURE 23

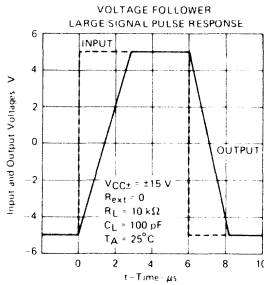


FIGURE 24

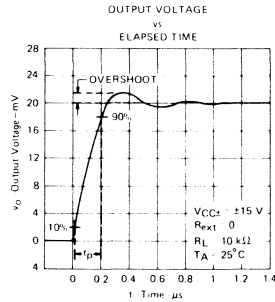
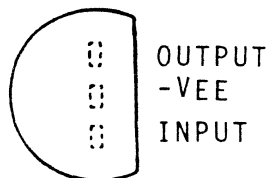


FIGURE 25

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

- 3 lead LP (TO-92) package
- Minimum supply current . . . 200 $\mu$ A
- Wide input/output voltage range
- Low input bias current
- Output short circuit protection
- High Impedence input . . . JFET input stage
- Internal frequency compensation
- Latch-up free operation

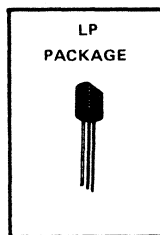
TOP VIEW



**description**

The TL068 is a JFET input unity gain amplifier featuring high input impedance, wide bandwidth, and low input bias current. A current sourcing load, such as a pull up resistor, is required for circuit operation.

The TL068 is characterized for operation over the commercial temperature range of 0°C to 70°C.



**DC characteristics (see test ckt) (25°C unless noted)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
$A_V$ Voltage Gain	$-V_{EE} = -15V, V_+ = 15V,$ $R_L = 10k\Omega$	.9990	.9997		V/V
$V_{IO}$ Offset Voltage	$I_L = 2mA$		3	15	mV
$I_{IB}$ Input Bias Current	$T_A = 25^\circ C$		30	400	pA
	$T_A = 70^\circ C$			10	nA
SVRR $\Delta V_{EE} / \Delta V_{IO}$	$-30 < -V_{EE} < -5V$	70	78		dB
ILRR $\Delta V_{IL} / \Delta I_L$	$0.5 < I_L < 0.5 mA$		2	4	mV/mA
$I_{EE}$ Minimum Supply Current			125	300	$\mu$ A
$I_{SC}$ Short Circuit Current			25		mA
$V_{IN}$ Input Voltage Range	$-V_{EE} = -15V, V_+ = 5V,$ $R_L = 10k\Omega$	+12	+13.5		V
		-11.5V	-12		

**AC Characteristics measured at  $R_L = 10k\Omega, C_L = 100pF, -V_{EE} = -15V, V_+ = 15V,$  and  $T_A = 25^\circ C.$  (See Test Ckt)**

PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNITS
Bandwidth			1		MHz
Slew rate	$V_O = \pm 10V$ Positive Edge		7		V/ $\mu$ S
		Negative Edge		100	
Rise time	$V_O = 100mV$		130		ns
Overshoot			20		%

**Absolute maximum ratings over operating free-air temperature range (unless otherwise noted).**

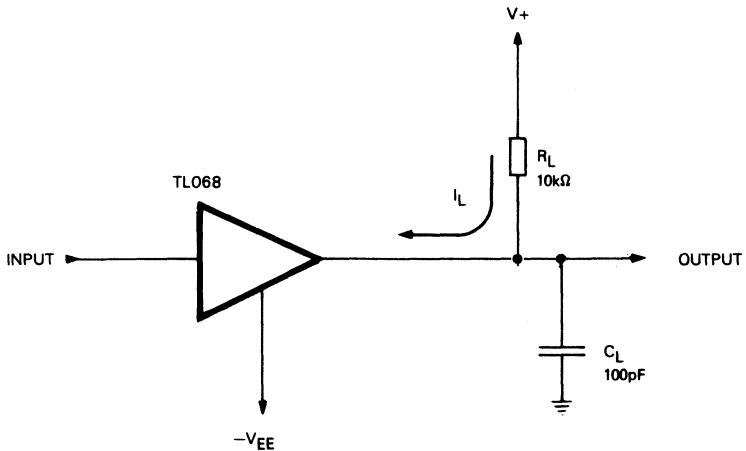
CONDITION	TL068	UNITS
Voltage from output to $-V_{EE}$	36	V
Voltage from input to $-V_{EE}$	36	V
Voltage from input to output	30	V
Duration of short circuit (see note 1)	Unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see note 2)	775	mW
Operating free-air temperature range	0 to 70	°C
Storage temperature range	-65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds	260	°C

- Notes: 1. The output may be shorted to any point as long as the voltage from output to  $V_{EE}$  does not exceed 36V. Temperature and/or  $-V_{EE}$  must be limited to ensure that the dissipation rating is not exceeded.  
 2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table.

**DISSIPATION DERATING TABLE**

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE $T_a$
LP	775mW	6.3,W/°C	25°C

TEST CIRCUIT



# LINEAR INTEGRATED CIRCUITS

# TYPES TL070, TL070A, TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL075 LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 12640, SEPTEMBER 1978

20 DEVICES COVER COMMERCIAL,  
INDUSTRIAL, AND MILITARY  
TEMPERATURE RANGES

- Low Noise . . .  $V_n = 18 \text{ nV}/\sqrt{\text{Hz}}$  Typ
- Low Harmonic Distortion . . . 0.01% Typ
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Low Power Consumption
- Latch-Up-Free Operation
- High Slew Rate . . .  $13 \text{ V}/\mu\text{s}$  Typ

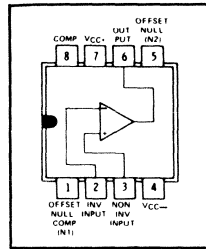
## description

The JFET-input operational amplifiers of the TL071 series are designed as low-noise versions of the TL081 series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL071 series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

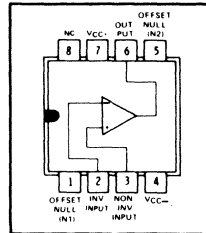
Device types with an "M" suffix are characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ , those with an "I" suffix are characterized for operation from  $-25^\circ\text{C}$  to  $85^\circ\text{C}$ , and those with a "C" suffix are characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

TL070, TL070A

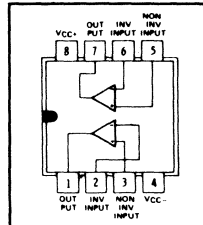
JG OR P DUAL-IN-LINE  
PACKAGE (TOP VIEW)



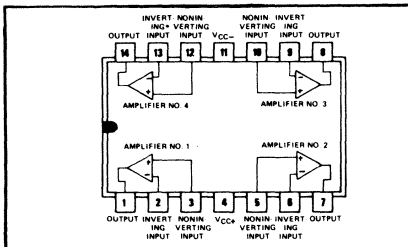
TL071, TL071A, TL071B  
JG OR P-DUAL-IN-LINE  
PACKAGE (TOP VIEW)



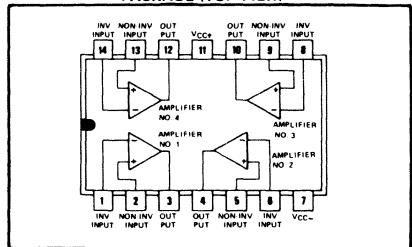
TL072, TL072A, TL072B  
JG OR P DUAL-IN-LINE  
PACKAGE (TOP VIEW)



TL074, TL074A, TL074B  
J OR N DUAL-IN-LINE  
PACKAGE (TOP VIEW)



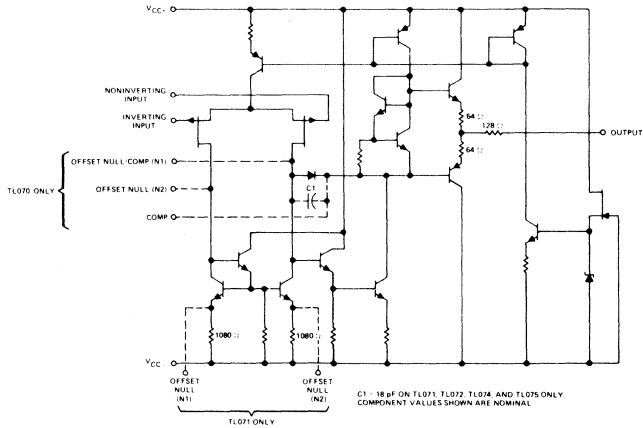
TL075  
N DUAL-IN-LINE  
PACKAGE (TOP VIEW)



# TYPES TL070, TL070A, TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL075

## LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL07_M	TL07_I	TL07_C TL07_AC TL07_BC	UNIT
Supply voltage, $V_{CC+}$ (see Note 1)		18	18	18	V
Supply voltage, $V_{CC-}$ (see Note 1)		-18	-18	-18	V
Differential input voltage (see Note 2)		$\pm 30$	$\pm 30$	$\pm 30$	V
Input voltage (see Notes 1 and 3)		$\pm 15$	$\pm 15$	$\pm 15$	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	J, JG, N, or P Package	680	680	680	mW
Operating free-air temperature range		-55 to 125	-25 to 85	0 to 70	°C
Storage temperature range		-65 to 150	-65 to 150	-65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG Package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package		260	260	°C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE $T_A$
J	680 mW	8.2 mW/°C	67°C
JG	680 mW	6.6 mW/°C	47°C
N	680 mW	9.2 mW/°C	76°C
P	680 mW	8.0 mW/°C	65°C

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TL070	TL071	TL072	TL074	TL075
TL07_M	JG	JG,	JG,	J	*
TL07_I	JG, P	JG, P	JG, P	J, N	*
TL07_C	JG, P	JG, P	JG, P	J, N	N
TL07_AC	JG, P	JG, P	JG, P	J, N	*
TL07_BC	*	JG, P	JG, P	J, N	*

\*These combinations are not defined by this data sheet.

# TYPES TL070, TL070A, TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL075 LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

electrical characteristics,  $V_{CC\pm} = \pm 15\text{ V}$

PARAMETER	TEST CONDITIONS†	TL07_M		TL07_I		TL07_C TL07_AC TL07_BC		UNIT					
		MIN	TYP	MAX	MIN	TYP	MAX		MIN	TYP	MAX		
$V_{IO}$	Input offset voltage	$R_S = 50\ \Omega$ , $T_A = 25^\circ\text{C}$	'70, '71, '72, '75‡		3	6	3	6	3	10	mV		
			'74		3	9	3	6	3	10			
		'70A, '71A, '72A, '74A								3		6	
		'71B, '72B, '74B								2		3	
		'70, '71, '72, '75‡				9		9				13	
		'74				15		9				13	
$\alpha V_{IO}$	Temperature coefficient of input offset voltage	$R_S = 50\ \Omega$ , $T_A = \text{full range}$			10		10		10		$\mu\text{V}/^\circ\text{C}$		
			'70A, '71A, '72A, '74A								7.5		
$I_{IO}$	Input offset current §	$R_S = 50\ \Omega$ , $T_A = 25^\circ\text{C}$	'70, '71, '72, '74, '75‡		5	100	5	100	5	100	pA		
			'70A, '71A, '72A, '74A									5	100
		'71B, '72B, '74B										5	100
		$T_A = \text{full range}$	'70, '71, '72, '74, '75‡				20		10			2	
			'70A, '71A, '72A, '74A									2	
		'71B, '72B, '74B										2	
$I_{IB}$	Input bias current §	$T_A = 25^\circ\text{C}$	'70, '71, '72, '74, '75‡		30	200	30	200	30	200	pA		
			'70A, '71A, '72A, '74A									30	200
		'71B, '72B, '74B										30	200
		$T_A = \text{full range}$	'70, '71, '72, '74, '75‡				50		20			7	
			'70A, '71A, '72A, '74A									7	
		'71B, '72B, '74B										7	
$V_{ICR}$	Common-mode input voltage range *	$T_A = 25^\circ\text{C}$	'70, '71, '72, '74, '75‡		$\pm 11$	$\pm 12$	$\pm 11$	$\pm 12$	$\pm 10$	$\pm 11$	V		
			'70A, '71A, '72A, '74A									$\pm 11$	$\pm 12$
'71B, '72B, '74B										$\pm 11$	$\pm 12$		
$V_{OPP}$	Maximum peak-to-peak output voltage swing	$T_A = 25^\circ\text{C}$ , $R_L = 10\ \text{k}\Omega$			24	27	24	27	24	27	V		
			$R_L \geq 10\ \text{k}\Omega$				24		24				
		$T_A = \text{full range}$	$R_L \geq 2\ \text{k}\Omega$				20	24	20	24		20	24
'70, '71, '72, '74, '75‡					50	200	50	200	25	200			
$A_{VD}$	Large-signal differential voltage amplification	$R_L \geq 2\ \text{k}\Omega$ , $V_O = +10\ \text{V}$ , $T_A = 25^\circ\text{C}$	'70A, '71A, '72A, '74A						50	200	V/mV		
			'71B, '72B, '74B									50	200
		$R_L \geq 2\ \text{k}\Omega$ , $V_O = +10\ \text{V}$ , $T_A = \text{full range}$	'70, '71, '72, '74, '75‡				25		25			15	
			'70A, '71A, '72A, '74A									25	
		'71B, '72B, '74B										25	
		$B_1$	Unity-gain bandwidth	$T_A = 25^\circ\text{C}$ , $R_L = 10\ \text{k}\Omega$			3		3			3	
$r_i$	Input resistance	$T_A = 25^\circ\text{C}$			$10^{12}$		$10^{12}$		$10^{12}$		$\Omega$		
CMRR	Common-mode rejection ratio	$R_S \leq 10\ \text{k}\Omega$ , $T_A = 25^\circ\text{C}$	'70, '71, '72, '74, '75‡		80	86	80	86	70	76	dB		
			'70A, '71A, '72A, '74A									80	86
		'71B, '72B, '74B											80
$K_{SVR}$	Supply voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$R_S \leq 10\ \text{k}\Omega$ , $T_A = 25^\circ\text{C}$	'70, '71, '72, '74, '75‡		80	86	80	86	70	76	dB		
			'70A, '71A, '72A, '74A									80	86
		'71B, '72B, '74B											80
$I_{CC}$	Supply current (per amplifier)	No load, $T_A = 25^\circ\text{C}$			1.4	2.5	1.4	2.5	1.4	2.5	mA		
$V_{O1}/V_{O2}$	Channel separation	$A_{VD} = 100$ , $T_A = 25^\circ\text{C}$			120		120		120		dB		

† All characteristics are specified under open-loop conditions unless otherwise noted. Full range for  $T_A$  is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for TL07\_M,  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  for TL07\_I, and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for TL07\_C, TL07\_AC, and TL07\_BC.

‡ Types TL075I and TL075M are not defined by this data sheet.

§ Input bias currents of a FET input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.

\* The  $V_{ICR}$  limits are directly linked volt-for-volt to supply voltage, viz the limit is 4 volts less than  $|V_{CC\pm}|$ .

# TYPES TL070, TL070A, TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL075

## LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , See Figure 1		13		$\text{V}/\mu\text{s}$
$t_r$	Rise time	$V_I = 20\text{ mV}$ , $R_L = 2\text{ k}\Omega$ , See Figure 1		0.1		$\mu\text{s}$
	Overshoot factor	$C_L = 100\text{ pF}$ , See Figure 1		10%		
$V_n$	Equivalent input noise voltage	$R_S = 100\ \Omega$ , $f = 1\text{ kHz}$		18		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ Hz to } 10\text{ kHz}$		4		$\mu\text{V}$
$I_n$	Equivalent input noise current	$R_S = 100\ \Omega$ , $f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$V_{O(\text{rms})} = 10\text{ V}$ , $R_L \geq 2\text{ k}\Omega$ , $R_S \leq 1\text{ k}\Omega$ , $f = 1\text{ kHz}$		0.01%		

### PARAMETER MEASUREMENT INFORMATION

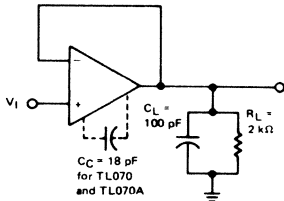


FIGURE 1—UNITY-GAIN AMPLIFIER

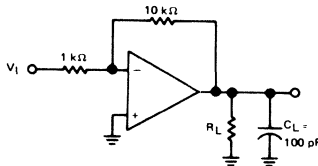


FIGURE 2—GAIN-OF-10 INVERTING AMPLIFIER

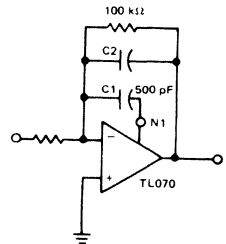


FIGURE 3—FEED-FORWARD COMPENSATION

### INPUT OFFSET VOLTAGE NULL CIRCUITS

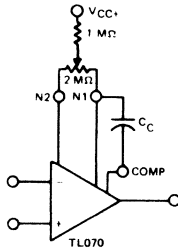


FIGURE 4

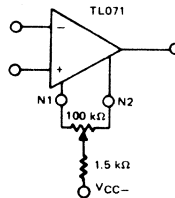


FIGURE 5



# TYPES TL070, TL070A, TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL075

## LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

### TYPICAL CHARACTERISTICS†

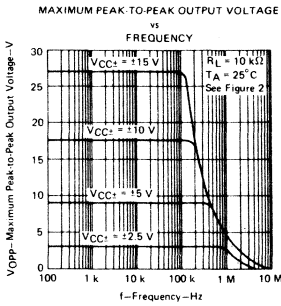


FIGURE 6

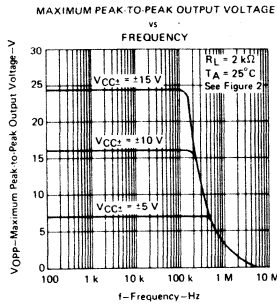


FIGURE 7

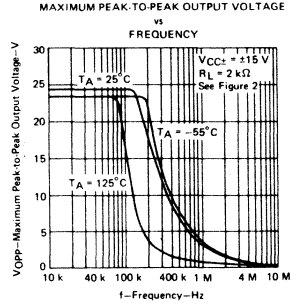


FIGURE 8

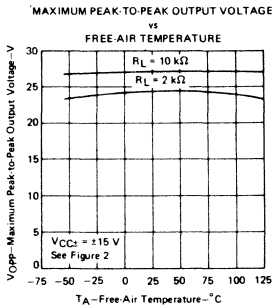


FIGURE 9

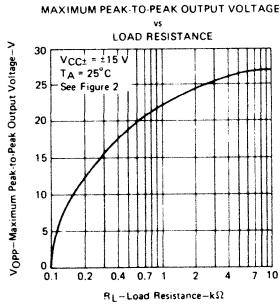


FIGURE 10

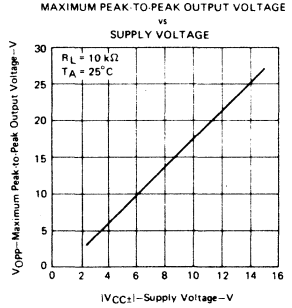


FIGURE 11

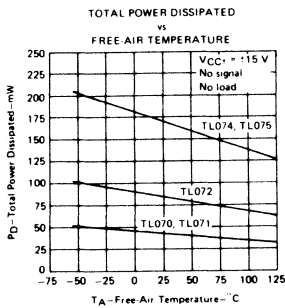


FIGURE 12

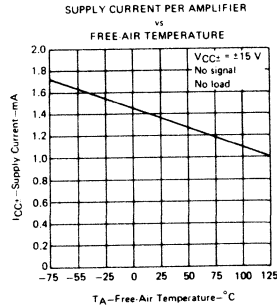


FIGURE 13

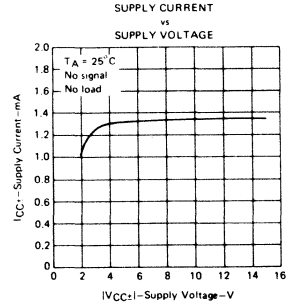


FIGURE 14

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 18-pF compensation capacitor is used with TL070 and TL070A.

# TYPES TL070, TL070A, TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL075

## LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

### TYPICAL CHARACTERISTICS<sup>1</sup>

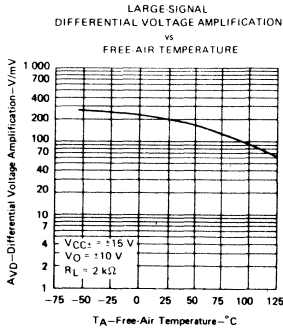


FIGURE 15

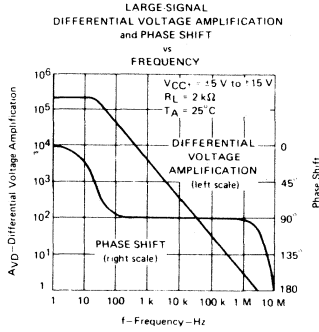


FIGURE 16

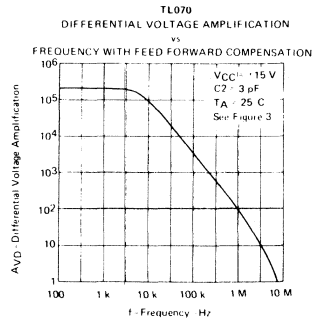


FIGURE 17

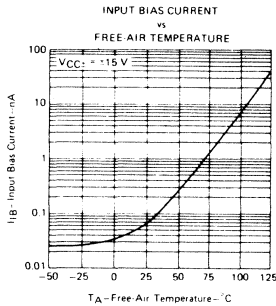


FIGURE 18

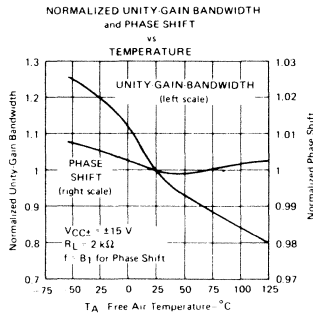


FIGURE 19

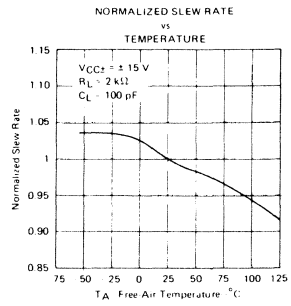


FIGURE 20

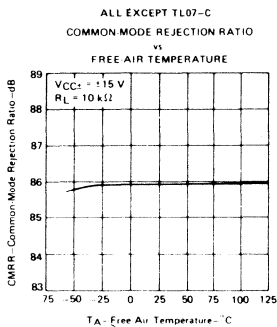


FIGURE 21

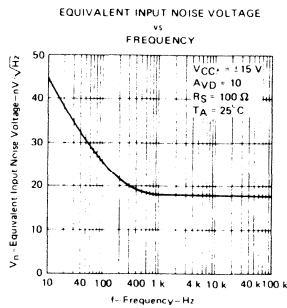


FIGURE 22

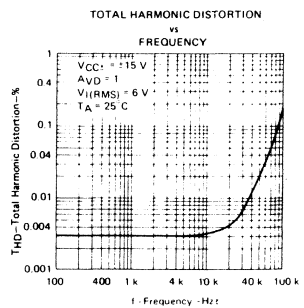


FIGURE 23

<sup>1</sup>Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 18-pF compensation capacitor is used with TL070 and TL070A.

# TYPES TL070, TL070A, TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL075 LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

## TYPICAL CHARACTERISTICS†

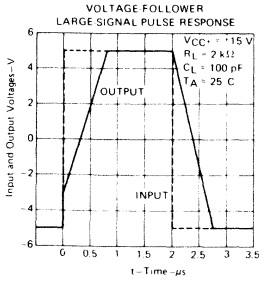


FIGURE 24

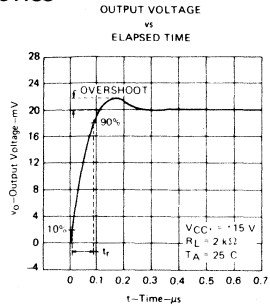


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 18-pF compensation capacitor is used with TL070 and TL070A.

## Packages and pin assignments

TL080	TL081, TL071, TL061	TL082, TL072, TL062	
<p><b>JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)</b></p>	<p><b>JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)</b></p>	<p><b>JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)</b></p>	<p><b>8-PIN DUAL-IN-LINE PACKAGES</b></p>
<p><b>TL083</b></p> <p><b>J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)</b></p>	<p><b>TL084, TL074, TL064</b></p> <p><b>J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)</b></p>	<p><b>TL085, TL075</b></p> <p><b>J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)</b></p>	<p><b>14-PIN DUAL-IN-LINE PACKAGES</b></p>

NC — NO INTERNAL CONNECTION

# LINEAR INTEGRATED CIRCUITS

# TYPES TL080 THRU TL085, TL080A THRU TL084A, TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 12484, FEBRUARY 1977- REVISED JUNE 1978

24 DEVICES COVER COMMERCIAL,  
INDUSTRIAL, AND MILITARY  
TEMPERATURE RANGES

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL080, TL080A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/ $\mu$ s Typ

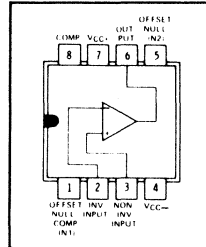
### description

The TL081 JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL081 Family.

Device types with an "M" suffix are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , those with an "I" suffix are characterized for operation from  $-25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , and those with a "C" suffix are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

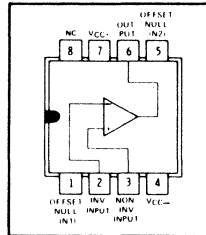
TL080, TL080A

JG OR P DUAL-IN-LINE  
PACKAGE (TOP VIEW)



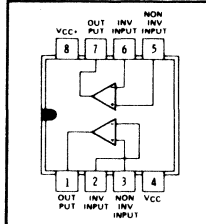
TL081, TL081A, TL081B

JG OR P DUAL-IN-LINE  
PACKAGE (TOP VIEW)

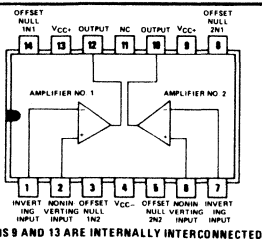


TL082, TL082A, TL082B

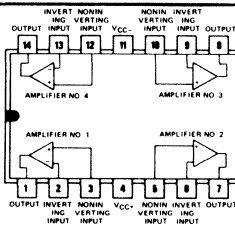
JG OR P DUAL-IN-LINE  
PACKAGE (TOP VIEW)



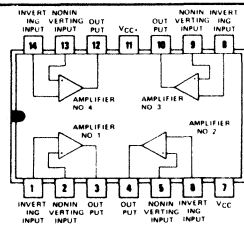
TL083, TL083A  
J OR N DUAL-IN-LINE  
PACKAGE (TOP VIEW)



TL084, TL084A, TL084B  
J OR N DUAL-IN-LINE  
PACKAGE (TOP VIEW)



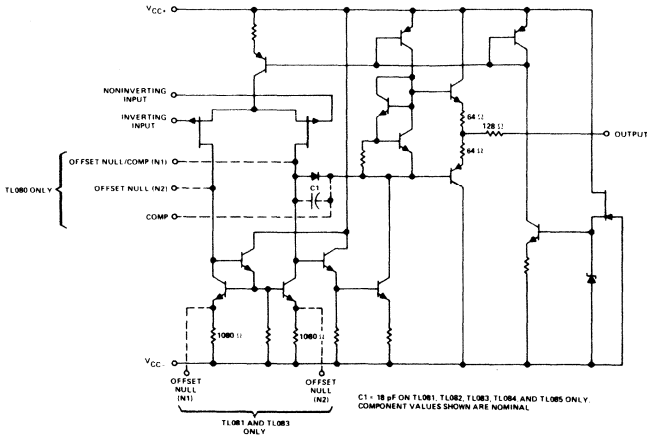
TL085  
N DUAL-IN-LINE  
PACKAGE (TOP VIEW)



NC - No internal connection

# TYPES TL080 THRU TL085, TL080A THRU TL084A, TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL08_M	TL08_I	TL08_C TL08_AC TL08_BC	UNIT
Supply voltage, $V_{CC+}$ (see Note 1)		18	18	18	V
Supply voltage, $V_{CC-}$ (see Note 1)		-18	-18	-18	V
Differential input voltage (see Note 2)		$\pm 30$	$\pm 30$	$\pm 30$	V
Input voltage (see Notes 1 and 3)		$\pm 15$	$\pm 15$	$\pm 15$	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (See Note 5)	J, JG, N, or P Package	680	680	680	mW
Operating free-air temperature range		-55 to 125	-25 to 85	0 to 70	°C
Storage temperature range		-65 to 150	-65 to 150	-65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG Package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package		260	260	°C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free air temperature, refer to Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE $T_A$
J	680 mW	8.2 mW/°C	67°C
JG	680 mW	6.6 mW/°C	47°C
N	680 mW	9.2 mW/°C	76°C
P	680 mW	8.0 mW/°C	65°C

DEVICE TYPES, SUFFIX VERSIONS, AND PACKAGES

	TL080	TL081	TL082	TL083	TL084	TL085
TL08_M	JG	JG	JG	J	J	*
TL08_I	JG, P	JG, P	JG, P	J, N	J, N	*
TL08_C	JG, P	JG, P	JG, P	J, N	J, N	N
TL08_AC	JG, P	JG, P	JG, P	J, N	J, N	*
TL08_BC	*	JG, P	JG, P	*	J, N	*

\* These combinations are not defined by this data sheet.

# TYPES TL080 THRU TL085, TL080A THRU TL084A, TL081B, TL082B, TL084B

## JFET-INPUT OPERATIONAL AMPLIFIERS

electrical characteristics,  $V_{CC\pm} = \pm 15$  V

PARAMETER	TEST CONDITIONS†		TL08_M		TL08_I		TL08_C TL08_AC TL08_BC		UNIT
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
$V_{IO}$ Input offset voltage	$R_S = 50 \Omega$ , $T_A = 25^\circ\text{C}$	TL08_‡	3	6	3	6	5	15	mV
		TL08_A‡					3	6	
	'81B,'82B,'84B					2	3		
	TL08_‡		9		9		20		
$R_S = 50 \Omega$ , $T_A = \text{full range}$	TL08_A‡						7.5		
	'81B,'82B,'84B						5		
$\alpha V_{IO}$ Temperature coefficient of input offset voltage	$R_S = 50 \Omega$ , $T_A = \text{full range}$		10		10		10	$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$ Input offset current §	$T_A = 25^\circ\text{C}$	TL08_‡	5	100	5	100	5	200	pA
		TL08_A‡					5	100	
		'81B,'82B,'84B					5	100	
	$T_A = \text{full range}$	TL08_‡		20		10		5	nA
TL08_A‡							3		
$I_{IB}$ Input bias current §	$T_A = 25^\circ\text{C}$	TL08_‡		30 200		30 200		30 400	pA
		TL08_A‡						30 200	
		'81B,'82B,'84B						30 200	
	$T_A = \text{full range}$	TL08_‡		50		20		10	nA
		TL08_A‡						7	
		'81B,'82B,'84B						7	
$V_{ICR}$ Common-mode input voltage range●	$T_A = 25^\circ\text{C}$	TL08_‡	$\pm 11$	$\pm 12$	$\pm 11$	$\pm 12$	$\pm 10$	$\pm 11$	V
		TL08_A‡					$\pm 11$	$\pm 12$	
		'81B,'82B,'84B					$\pm 11$	$\pm 12$	
$V_{OPP}$ Maximum peak-to-peak output voltage swing	$T_A = 25^\circ\text{C}$	$R_L = 10 \text{ k}\Omega$	24	27	24	27	24	27	V
	$T_A = \text{full range}$	$R_L \geq 10 \text{ k}\Omega$	24		24		24		
		$R_L \geq 2 \text{ k}\Omega$	20	24	20	24	20	24	
$A_{VD}$ Large-signal differential voltage amplification	$R_L \geq 2 \text{ k}\Omega$ , $V_O = \pm 10 \text{ V}$ , $T_A = 25^\circ\text{C}$	TL08_‡	50	200	50	200	25	200	V/mV
		TL08_A‡					50	200	
	'81B,'82B,'84B					50	200		
	$R_L \geq 2 \text{ k}\Omega$ , $V_O = \pm 10 \text{ V}$ , $T_A = \text{full range}$	TL08_‡	25		25		15		
		TL08_A‡					25		
	'81B,'82B,'84B					25			
$B_1$ Unity-gain bandwidth	$T_A = 25^\circ\text{C}$		3		3		3	MHz	
$r_i$ Input resistance	$T_A = 25^\circ\text{C}$		$10^{12}$		$10^{12}$		$10^{12}$	$\Omega$	
CMRR Common-mode rejection ratio	$R_S \leq 10 \text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	TL08_‡	80	86	80	86	70	76	dB
		TL08_A‡					80	86	
		'81B,'82B,'84B					80	86	
$k_{SVR}$ Supply voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$R_S \leq 10 \text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	TL08_‡	80	86	80	86	70	76	dB
		TL08_A‡					80	86	
		'81B,'82B,'84B					80	86	
$I_{CC}$ Supply current (per amplifier)	No load, $T_A = 25^\circ\text{C}$	No signal,	1.4	2.8	1.4	2.8	1.4	2.8	mA
$V_{O1}/V_{O2}$ Channel separation	$A_{VD} = 100$ , $T_A = 25^\circ\text{C}$		120		120		120	dB	

† All characteristics are specified under open-loop conditions unless otherwise noted. Full range for  $T_A$  is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for TL08\_M  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  for TL08\_I, and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for TL08\_C, TL08\_AC, and TL08\_BC.

‡ Types TL085I, and TL085M are not defined by this data sheet.

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

● The  $V_{ICR}$  limits are directly linked volt for volt to supply voltage, viz the limit is 4 volts less than  $|V_{CC\pm}|$ .

# TYPES TL080 THRU TL085, TL080A THRU TL084A, TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

operating characteristics,  $V_{CC} \pm = \pm 15 \text{ V}$ ,  $T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$S_R$ Slew rate at unity gain	$V_I = 10 \text{ V}$ , $R_L = 2 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$ , See Figure 1		13		$\text{V}/\mu\text{s}$
$t_r$ Rise time	$V_I = 20 \text{ mV}$ , $R_L = 2 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$ , See Figure 1		0.1		$\mu\text{s}$
Overshoot factor			10%		
$V_n$ Equivalent input noise voltage	$R_S = 100 \Omega$ , $f = 1 \text{ kHz}$		25		$\text{nV}/\sqrt{\text{Hz}}$

## PARAMETER MEASUREMENT INFORMATION

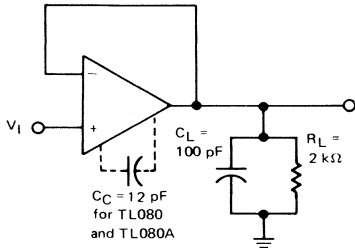


FIGURE 1—UNITY-GAIN AMPLIFIER

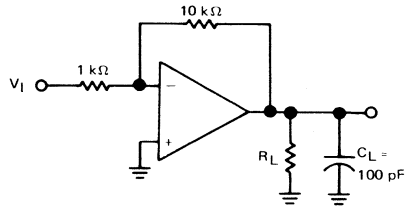


FIGURE 2—GAIN-OF-10 INVERTING AMPLIFIER

## INPUT OFFSET VOLTAGE NULL CIRCUITS

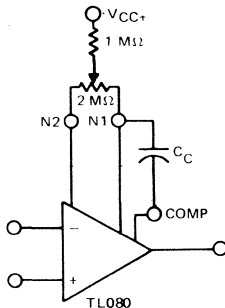


FIGURE 3

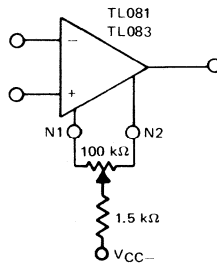


FIGURE 4

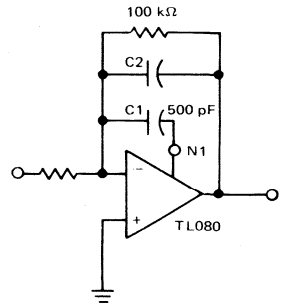


FIGURE 5

# TYPES TL080 THRU TL085, TL080A THRU TL084A, TL081B, TL082B, TL084B

## JFET-INPUT OPERATIONAL AMPLIFIERS

### TYPICAL CHARACTERISTICS†

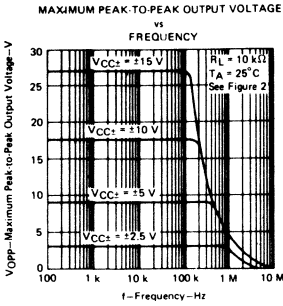


FIGURE 6

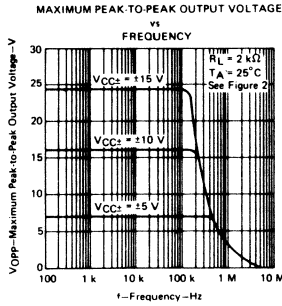


FIGURE 7

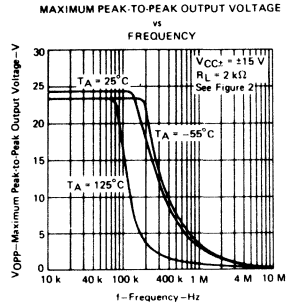


FIGURE 8

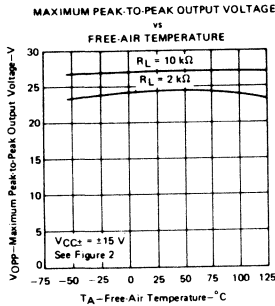


FIGURE 9

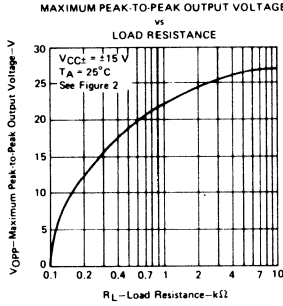


FIGURE 10

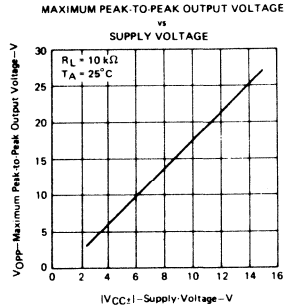


FIGURE 11

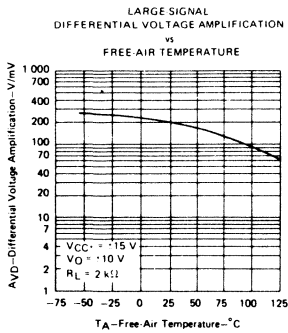


FIGURE 12

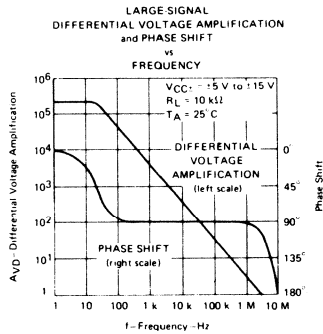


FIGURE 13

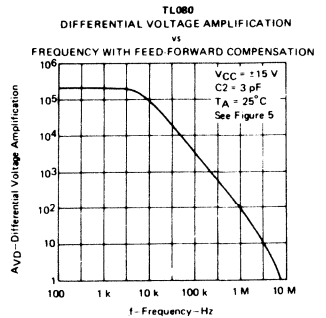


FIGURE 14

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.



# TYPES TL080 THRU TL085, TL080A THRU TL084A, TL081B, TL082B, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

## TYPICAL CHARACTERISTICS†

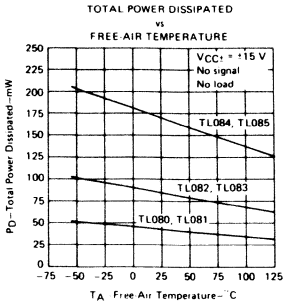


FIGURE 15

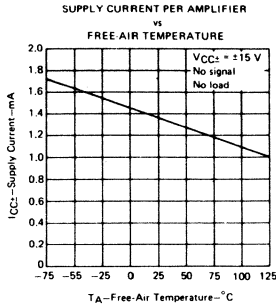


FIGURE 16

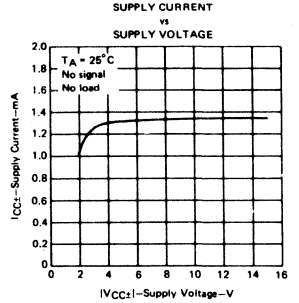


FIGURE 17

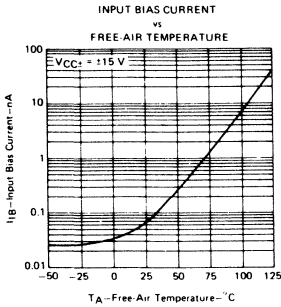


FIGURE 18

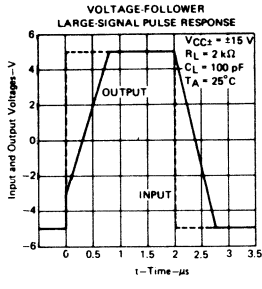


FIGURE 19

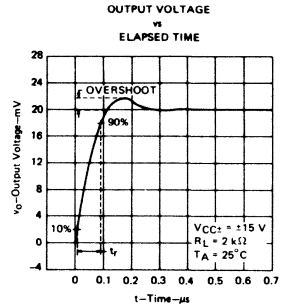


FIGURE 20

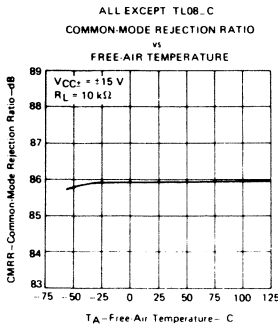


FIGURE 21

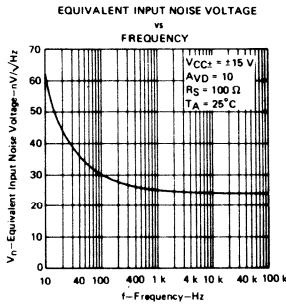


FIGURE 22

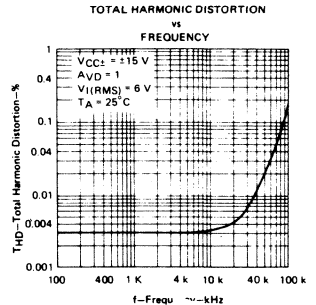


FIGURE 23

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

# LINEAR INTEGRATED CIRCUITS

## TYPES TL087, TL088, TL287, TL288 JFET-INPUT OPERATIONAL AMPLIFIERS

BULLETIN NO. DL S 12642, MARCH 1979

- Low Input Offset Voltage . . . 0.5 mV Max
- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/ $\mu$ s Typ

### description

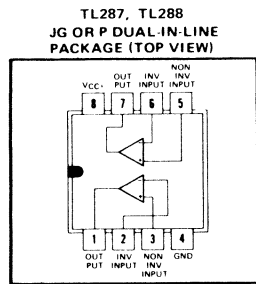
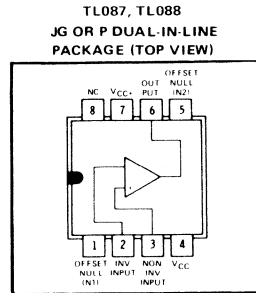
These JFET-input operational amplifiers incorporate well-matched high-voltage JFET and bipolar transistors in a monolithic integrated circuit. They feature low input offset voltage, high slew rate, low input bias and offset current, and low temperature coefficient of input offset voltage. Offset-voltage adjustment is provided for the TL087 and TL088.

Device types with an "M" suffix are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , those with "I" suffix are characterized for operation from  $-25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , and those with a "C" suffix are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL087M TL287M	TL087I TL088I TL287I TL288I	TL087C TL088C TL287C TL288C	UNIT
Supply voltage, $V_{CC+}$ (see Note 1)	18	18	18	V
Supply voltage, $V_{CC-}$ (see Note 1)	-18	-18	-18	V
Differential input voltage (see Note 2)	$\pm 30$	$\pm 30$	$\pm 30$	V
Input voltage (see Notes 1 and 3)	$\pm 15$	$\pm 15$	$\pm 15$	V
Duration of output short circuit (see Note 4)	Unlimited	Unlimited	Unlimited	
Continuous total dissipation at (or below) $25^{\circ}\text{C}$ free-air temperature (see Note 5)	680	680	680	mW
Operating free-air temperature range	$-55$ to $125$	$-25$ to $85$	$0$ to $70$	$^{\circ}\text{C}$
Storage temperature range	$-65$ to $150$	$-65$ to $150$	$-65$ to $150$	$^{\circ}\text{C}$
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds	JG Package 300	300	300	$^{\circ}\text{C}$
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	P Package 300	260	260	$^{\circ}\text{C}$

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above  $25^{\circ}\text{C}$  free-air temperature, refer to Dissipation Derating Table.



NC - No internal connection

# TYPES TL087, TL088, TL287, TL288 JFET-INPUT OPERATIONAL AMPLIFIERS

electrical characteristics,  $V_{CC\pm} = \pm 15 \text{ V}$

PARAMETER	TEST CONDITIONS†		TL087M TL287M			TL0871 TL0881 TL2871 TL2881			TL087C TL088C TL287C TL288C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$R_S = 50 \Omega$ , $T_A = 25^\circ\text{C}$	TL087, TL287	0.1	0.5		0.1	0.5		0.1	0.5	mV	
		TL088, TL288				1	3		1	3		
	$R_S = 50 \Omega$ , $T_A = \text{full range}$	TL087, TL287		3			2			1.5		
		TL088, TL288					6			5		
$\alpha V_{IO}$ Temperature coefficient of input offset voltage	$R_S = 50 \Omega$ , $T_A = \text{full range}$		10			10			10	$\mu\text{V}/^\circ\text{C}$		
$I_{IO}$ Input offset current §	$T_A = 25^\circ\text{C}$		5	100		5	100		5	100	pA	
	$T_A = \text{full range}$			25			3			2	nA	
$I_{IB}$ Input bias current §	$T_A = 25^\circ\text{C}$		60	400		60	400		60	400	pA	
	$T_A = \text{full range}$			100			20			7	nA	
$V_{ICR}$ Common-mode input Voltage range	$T_A = 25^\circ\text{C}$		$V_{CC-} + 3.5$ to $V_{CC+}$			$V_{CC-} + 3.5$ to $V_{CC+}$			$V_{CC-} + 5$ to $V_{CC+}$		V	
$V_{OPP}$ Maximum peak-to-peak output voltage swing	$T_A = 25^\circ\text{C}$ , $T_A = \text{full range}$	$R_L = 10 \text{ k}\Omega$	24	27		24	27		24	27	V	
		$R_L \geq 10 \text{ k}\Omega$	24			24			24			
	$R_L \geq 2 \text{ k}\Omega$	20			20			20				
$A_{VD}$ Large-signal differential voltage amplification	$R_L \geq 2 \text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	$V_O = \pm 10 \text{ V}$	50	200		50	200		25	200	V/mV	
		$R_L \geq 2 \text{ k}\Omega$ , $T_A = \text{full range}$	25			25			15			
	$V_O = \pm 10 \text{ V}$											
$B_1$ Unity-gain bandwidth	$T_A = 25^\circ\text{C}$		3			3			3	MHz		
$r_i$ Input resistance	$T_A = 25^\circ\text{C}$		$10^{12}$			$10^{12}$			$10^{12}$	$\Omega$		
CMRR Common-mode rejection ratio	$R_S \leq 10 \text{ k}\Omega$ , $T_A = 25^\circ\text{C}$		80	95		80	95		70	95	dB	
$k_{SVR}$ Supply voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$R_S \leq 10 \text{ k}\Omega$ , $T_A = 25^\circ\text{C}$		80	95		80	95		70	95	dB	
$I_{CC}$ Supply Current (per amplifier)	No load, No signal, $T_A = 25^\circ\text{C}$		1.4	2.8		1.4	2.8		1.4	2.8	mA	

† All characteristics are specified under open-loop conditions unless otherwise noted. Full range for  $T_A$  is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for TL-87M;  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  for TL-81; and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for TL-82-C.

§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics,  $V_{CC\pm} = \pm 15 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Slew rate at unity gain	$V_I = 10 \text{ V}$ , $C_L = 100 \text{ pF}$ , $A_{VD} = 1$		13		$\text{V}/\mu\text{s}$
$t_r$ Rise time	$V_I = 20 \text{ mV}$ , $C_L = 100 \text{ pF}$ , $A_{VD} = 1$		0.1		$\mu\text{s}$
			10%		
$V_n$ Equivalent input noise voltage	$R_S = 100 \Omega$ , $f = 1 \text{ kHz}$		18		$\text{nV}/\sqrt{\text{Hz}}$

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE $T_A$
JG	680 mW	6.6 mW/ $^\circ\text{C}$	47 $^\circ\text{C}$
P	680 mW	8.0 mW/ $^\circ\text{C}$	65 $^\circ\text{C}$

# TYPES TL087, TL088, TL287, TL288

## JFET-INPUT OPERATIONAL AMPLIFIERS

### TYPICAL CHARACTERISTICS†

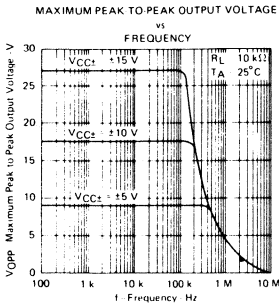


FIGURE 1

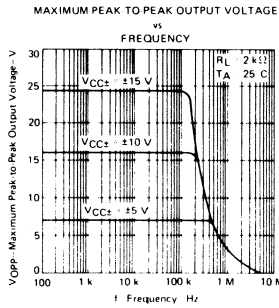


FIGURE 2

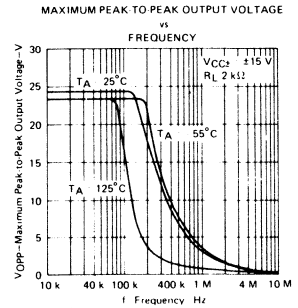


FIGURE 3

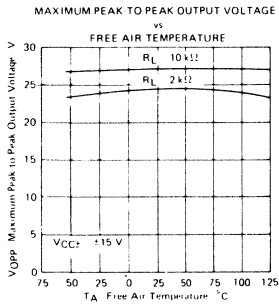


FIGURE 4

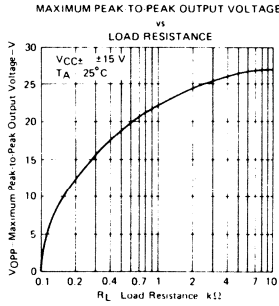


FIGURE 5

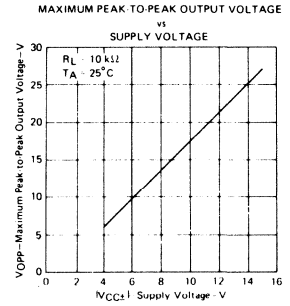


FIGURE 6

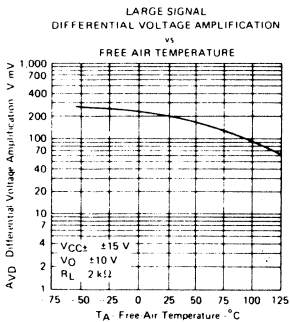


FIGURE 7

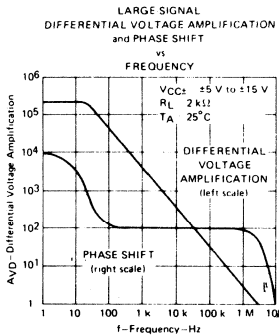


FIGURE 8

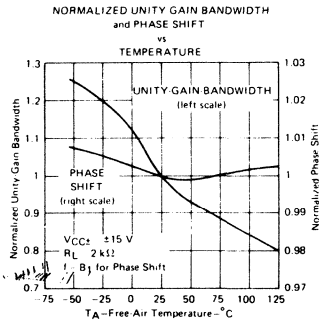


FIGURE 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TYPES TL087, TL088, TL287, TL288 JFET-INPUT OPERATIONAL AMPLIFIERS

## TYPICAL CHARACTERISTICS†

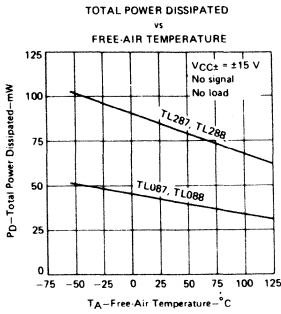


FIGURE 10

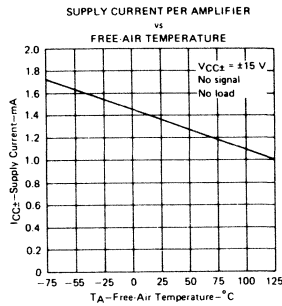


FIGURE 11

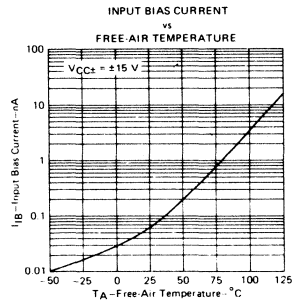


FIGURE 12

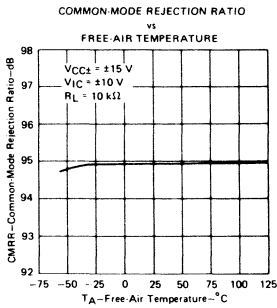


FIGURE 13

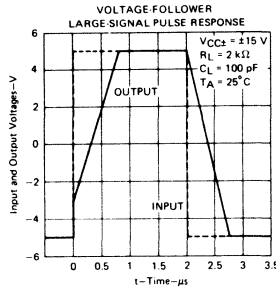


FIGURE 14

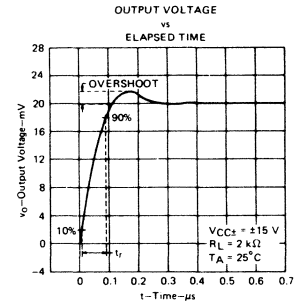


FIGURE 15

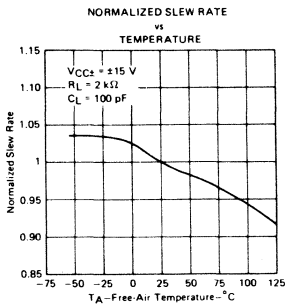


FIGURE 16

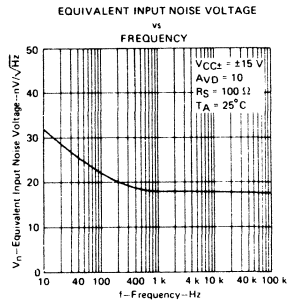


FIGURE 17

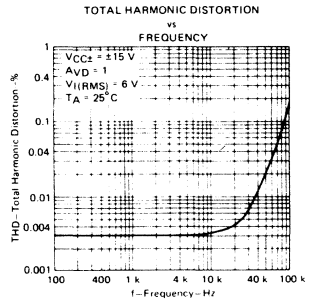


FIGURE 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





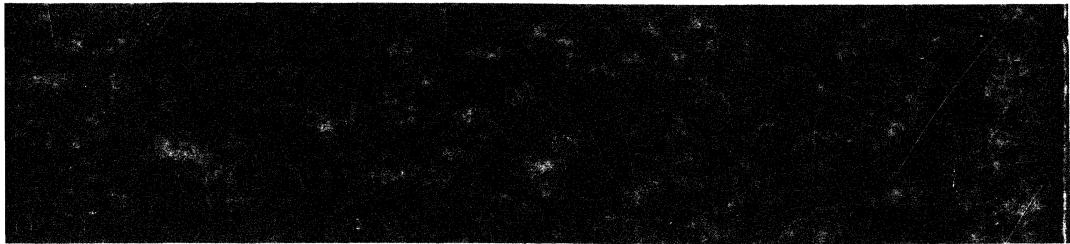












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